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HP Hurricane Tampa2 u-ATX Ver: 1.3

CPU:

INTEL-CFL LGA1151

System Chipset:

INTEL Z370

OnBoard Chipset:

HD Audio Codec: ALC3863

LAN: RTL8118ASH-CG

SIO: NCT6683D-T

Flash ROM: 16MB SPI Quad read

HDMI level shift: ASM1442k (support 4K x 2K)

Main Memory:

DDR4 (2400MHz) * 4 (2 DIMM per channel)

Expansion Slots:

PCI Express X16 Slot (8 lanes) * 2

M.2 2280 key-M (4 lanes) for SSD

M.2 2230 key A/E (1 lane) for WLAN

PWM:

IMVP8: ON Semiconductor NCP81203MNTXG
4Phase(VCCP)+1Phase(VCCGT)

Rear USB connector:

USB2.0 Type A *2

USB3.1 Gen1 Type A *2

USB3.1 Gen1 Type A *2+RJ45

Front USB pin header:

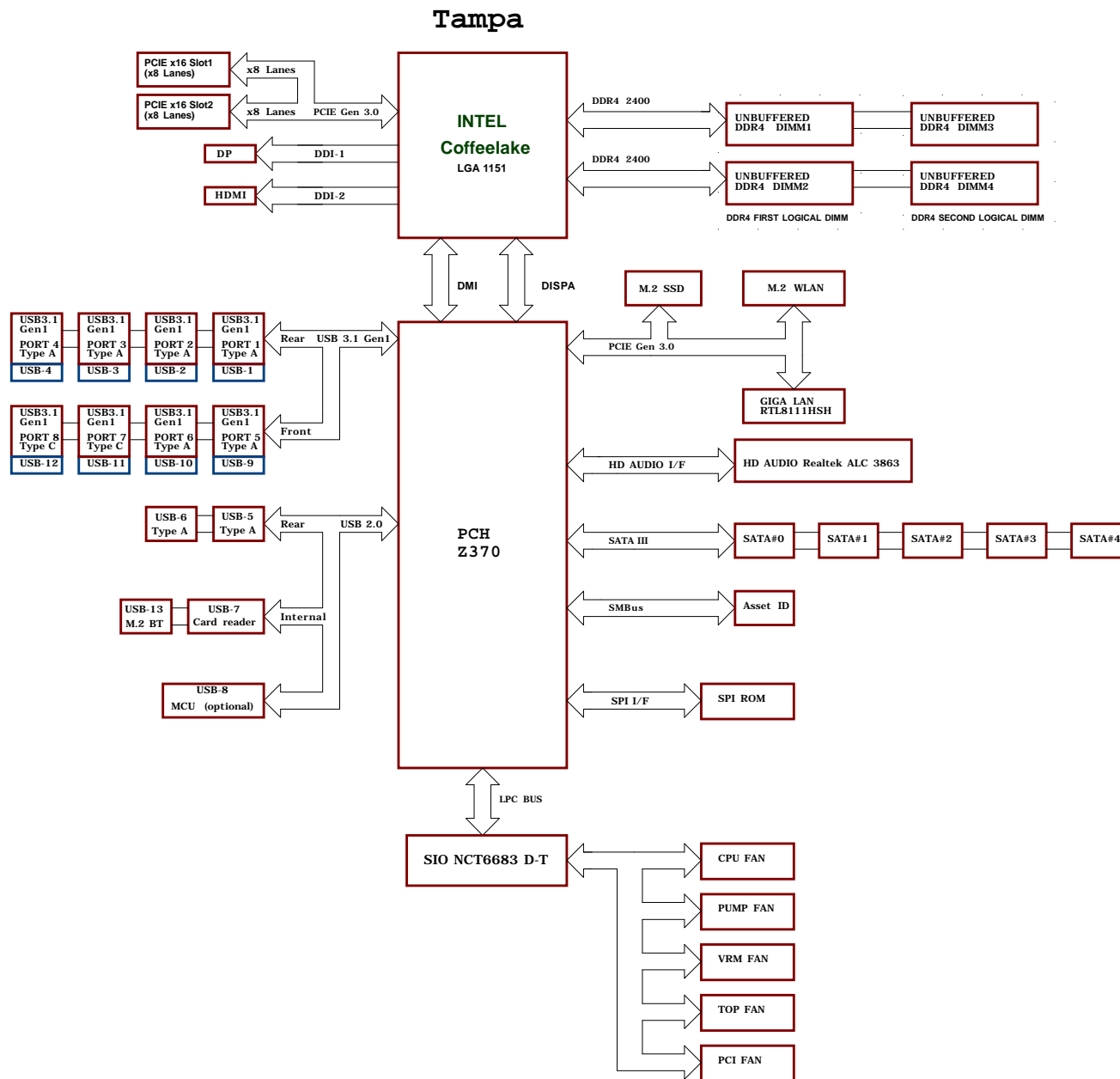
USB2.0 *1 for TIO card reader

USB3.1 Gen1 *2 for TIO Type A

USB3.1 Gen1 *2 for TIO Type C

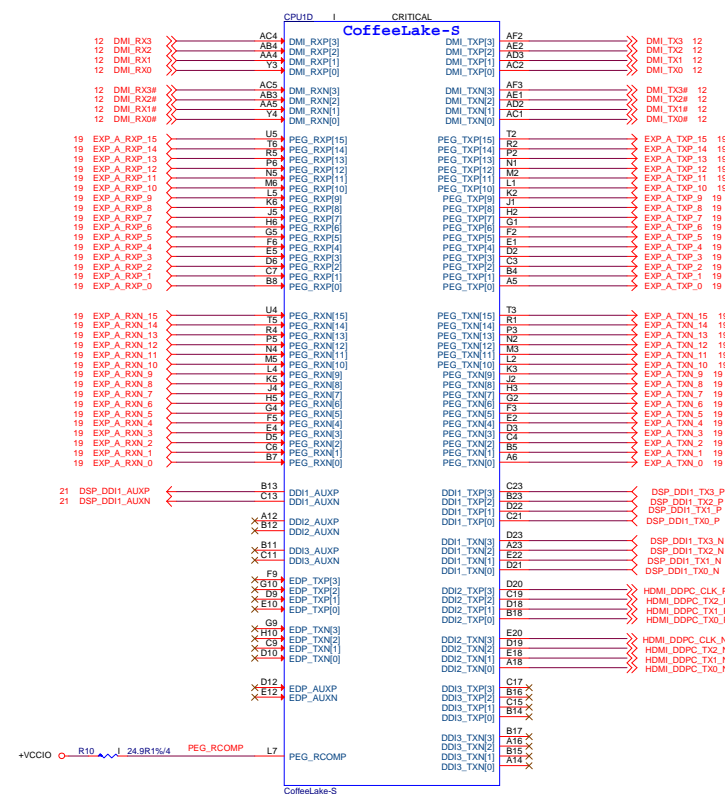
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CPU CFG	default is 1
CFG2	1
CFG6	1
CFG5	0
PCIe function	SLI
SLOT1	x8 lanes
SLOT2	x8 lanes

The processor's PCI Express® interface is a 16-lane (x16) port that can also be configured as multiple ports at narrower widths (see [Table 2-17](#), [Table 2-18](#)). The processor supports the configurations shown in the following table.

Table 2-17. PCI Express® Bifurcation and Lane Reversal Mapping

Differences	Link Width			Config. Signals			Lanes															
	0x1-2	0x3-4	0x5-6	CF [0]	CF [1]	CF [2]	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16	x16	N/A	N/A	1	0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1x16 Reversed	x16	N/A	N/A	1	0	0	0	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2
2x8	x8	x8	N/A	1	0	0	0	0	1	3	5	7	6	4	2	7	5	3	1	15	13	11
2x8 Reversed	x8	x8	N/A	1	0	0	0	0	0	15	13	11	9	7	5	3	1	15	13	11	9	7
1x8+2x4	x8	x4	x4	0	0	0	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1x8+2x4 Reversed	x8	x4	x4	0	0	0	0	0	0	15	14	13	12	11	10	9	8	7	6	5	4	3

Notes:


- For CPG bus further details, refer to Section 6.4.
- Support is also provided for narrow width and devices with lower number of lanes (that is, usage on x4 configuration), however further bifurcation is not supported.
- In case that more than one device is connected, the device with the highest lane count, should always be connected to the lower lanes, as follows:
 - Connect lane 0 of 1st device to Lane 0.
 - Connect lane 0 of 2nd device to Lane 8.
 - Connect lane 0 of 3rd device to Lane 16.

For example:


- When using 3x8 = 2x8, the 4 lane device must use lanes 0-7, and other 2 lanes device must use lanes 8-15.
- When using 2x8 + 3x4 = 1x16, the 4 lane device must use lanes 0-3, two lane device must use lanes 0-15, one lane device must use lanes 16-19.

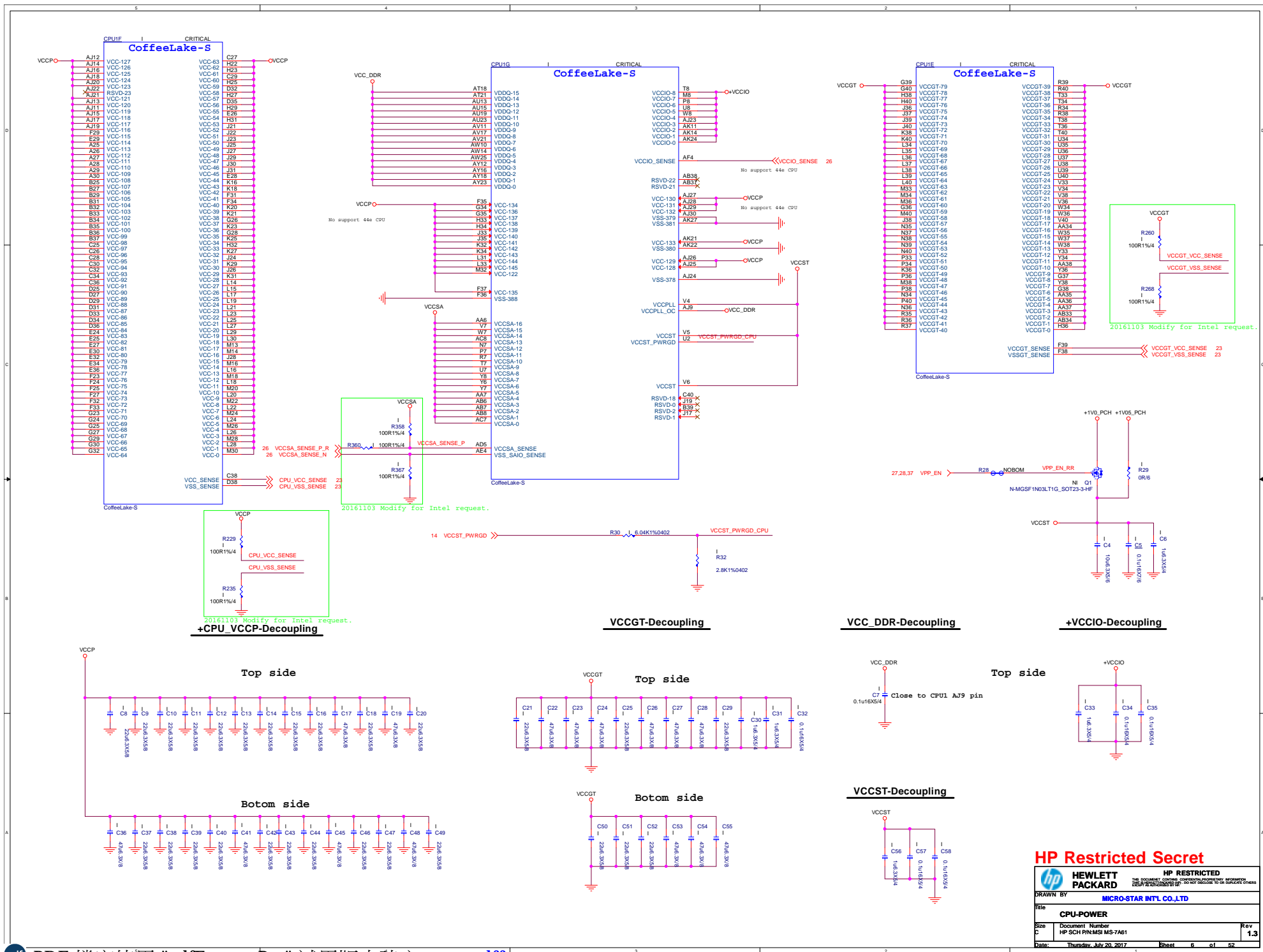
4. For reversal lanes, Example 1:

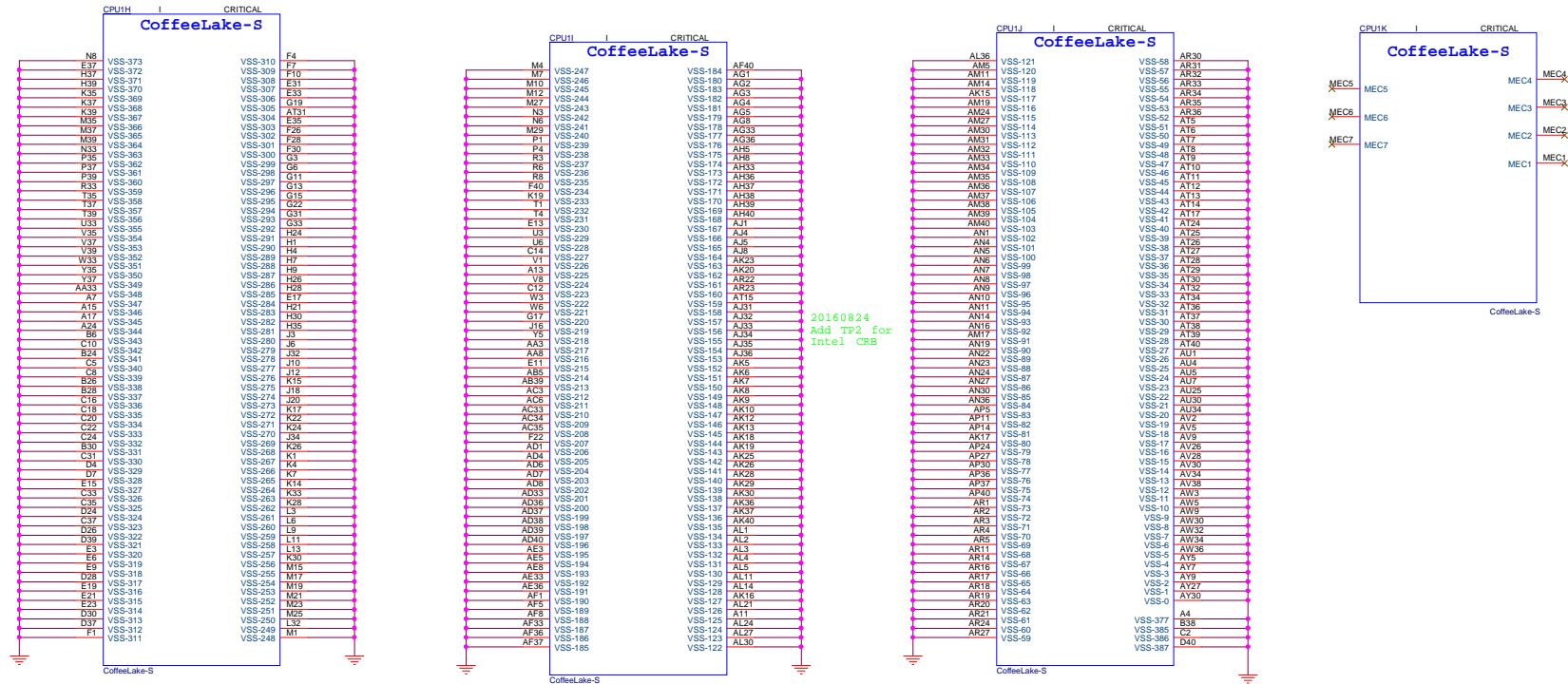
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The schematic shows two signal paths for DIMM voltage references. The top path, DIMM_VREF_A, starts from a source on the left, passes through a 2.2R1%0402-HF resistor (R24), then a 0.022u25X4 capacitor (C2), and finally a 24.91%4 resistor (R25) to ground. The bottom path, DIMM_DQ_VREF_B, follows a similar structure with a 2.2R1%0402-HF resistor (R26), a 0.022u25X4 capacitor (C3), and a 24.91%4 resistor (R27) to ground. The destination for both paths is labeled as DIMM_CA_CPU_VREF_A and DIMM_DQ_CPU_VREF_B on the right.

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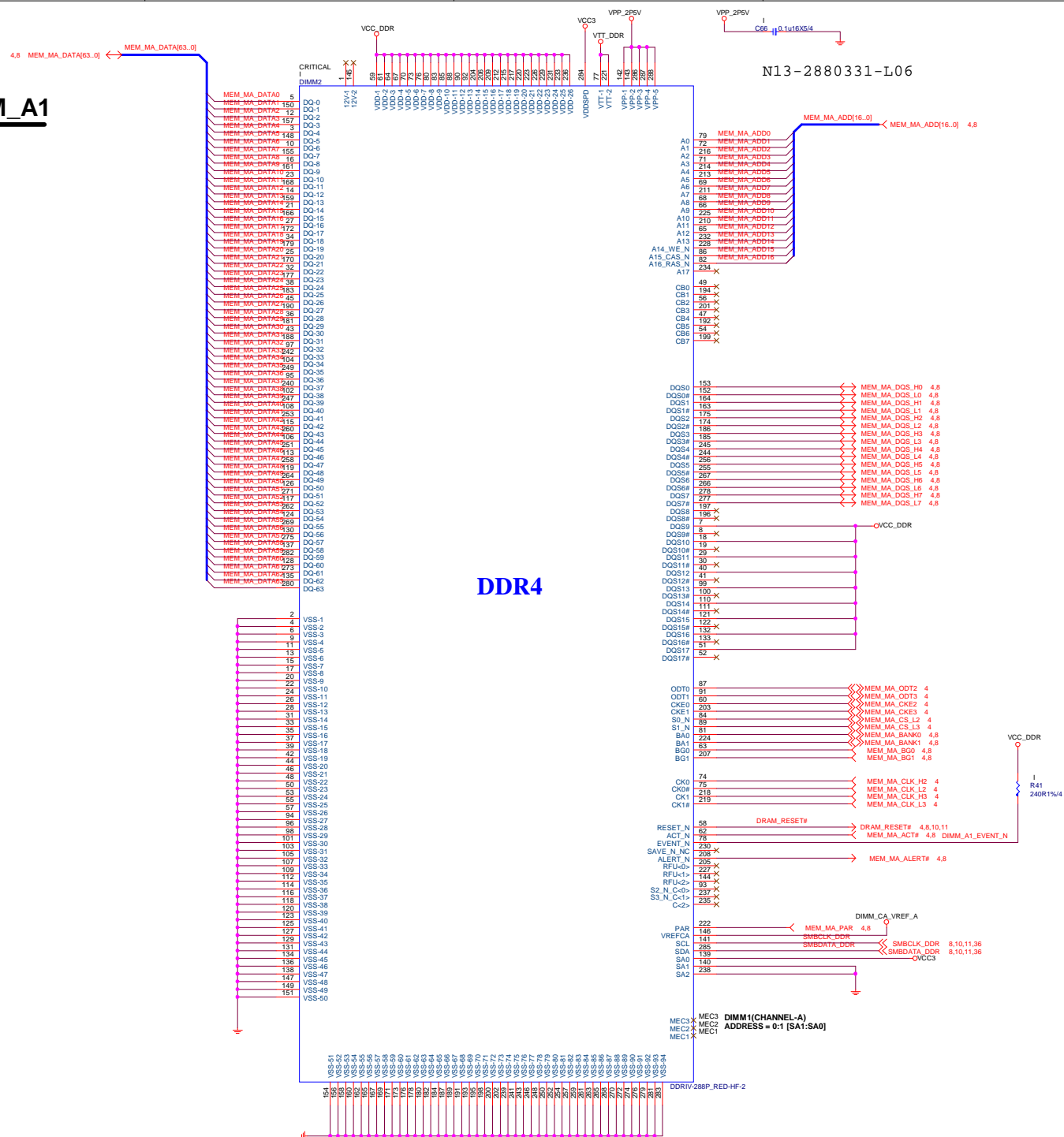


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DDR4 DIMM_A1



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DDR4 DIMM_B0

DDR4

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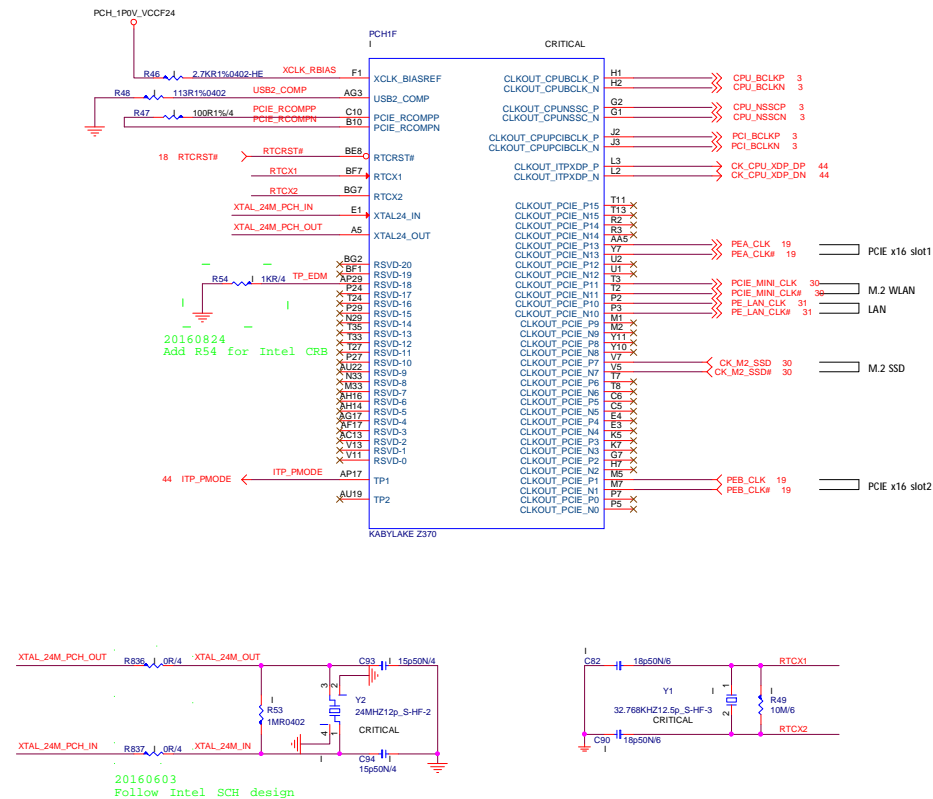
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DDR4 DIMM_B1

DDR4

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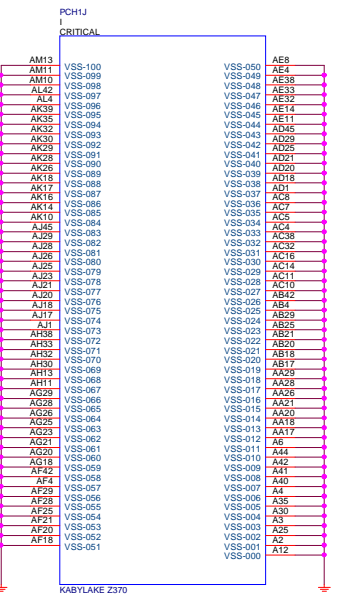
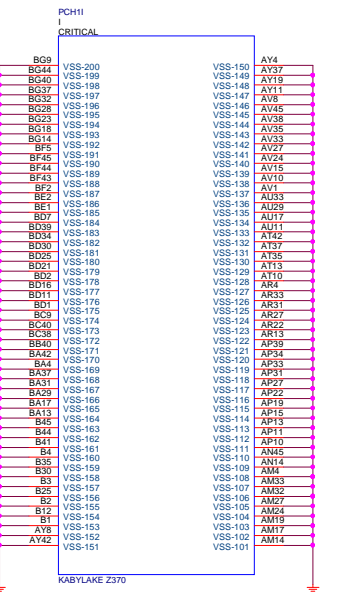
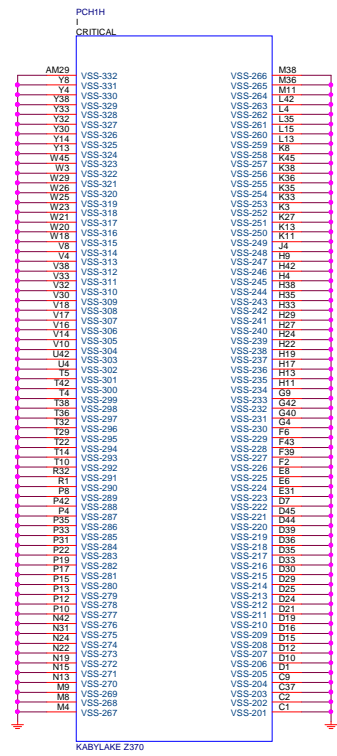


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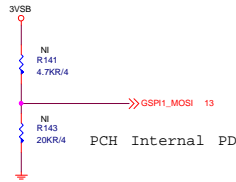


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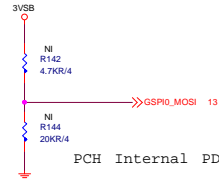
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GPP-B strapping

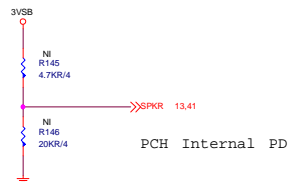
GSPII_MOSI	GPP_B22
LPC	1
SPI	0 **



GSPII0_MOSI	GPP_B18
Enable no boot	1
disable No boot	0 **



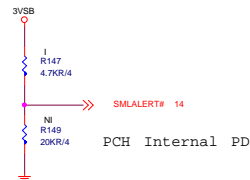
SWAP OVERRIDE STRAP	GPP_B14
ENABLE	1
DISABLE	0 **(default)



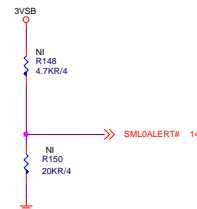
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GPP-C strapping

TLS	SMLALERT#
ENABLE	1 **
DISABLE	0



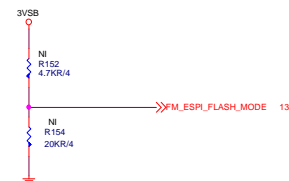
boot type	SMLOALERT#
ESPI	1
LPC	0 **(default)



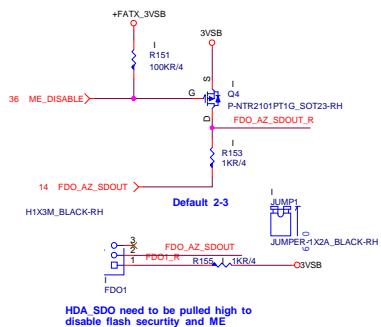
HW strapping

ESPI flash sharing mode

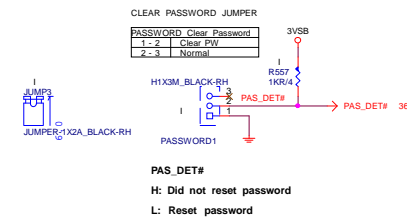
Slave	1
Master	0 **(default)



Flash Descriptor Override Header



PASSWORD DETECTION



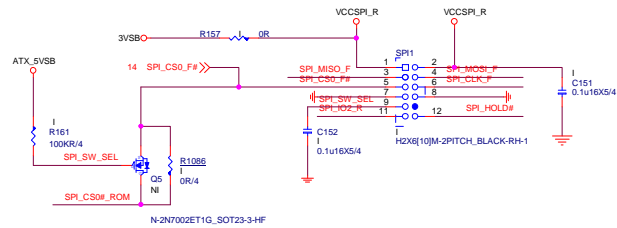
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SPI DEBUG PROT

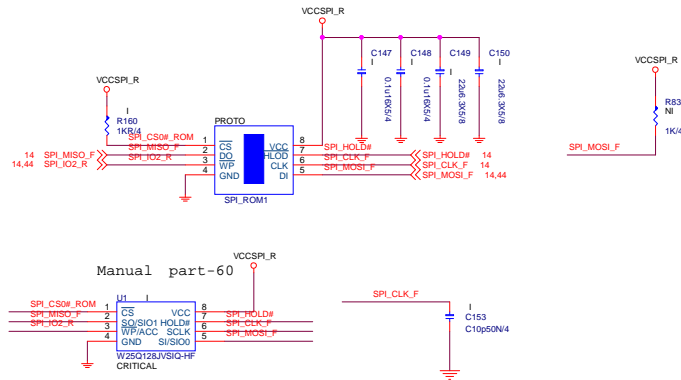
Close to SPI ROM

Part Number: N31-2061341-H06



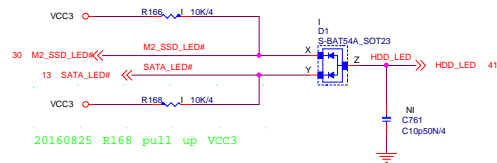
SPI FLASH ROM

Close to SB

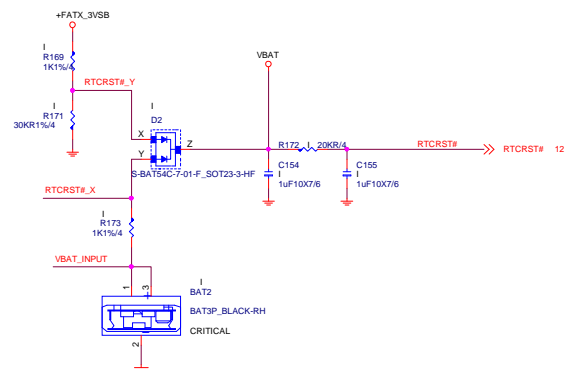


- 8M Main-Winbond M31-25Q6443-W03
- 8M AVL-MXIC M31-25L6482-M24
- 16M Main-Winbond M31-2512893-W03
- 16M AVL-MXIC M31-2512832-M24

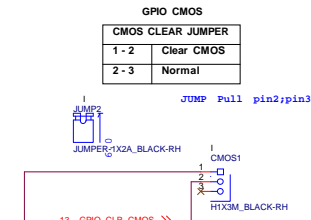
HDD LED



RTC



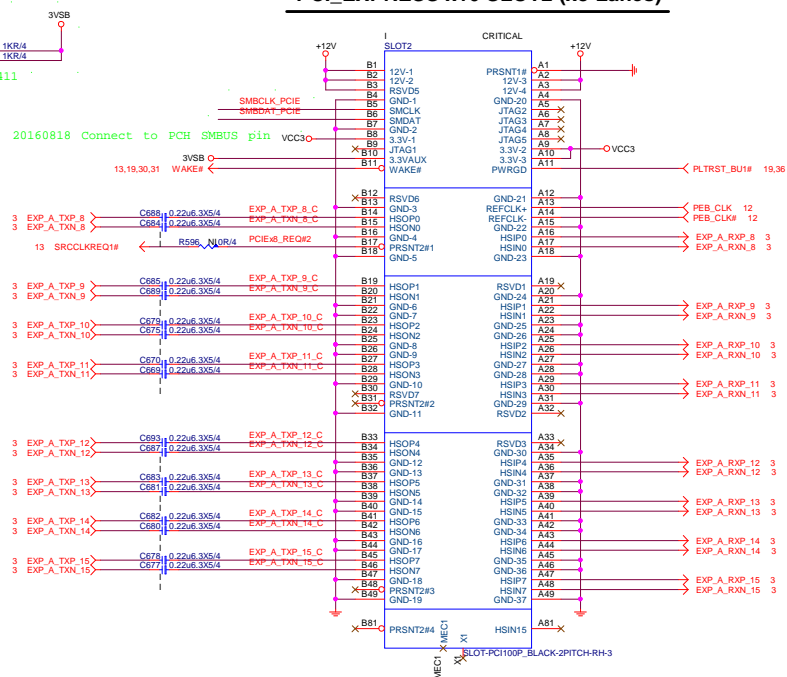
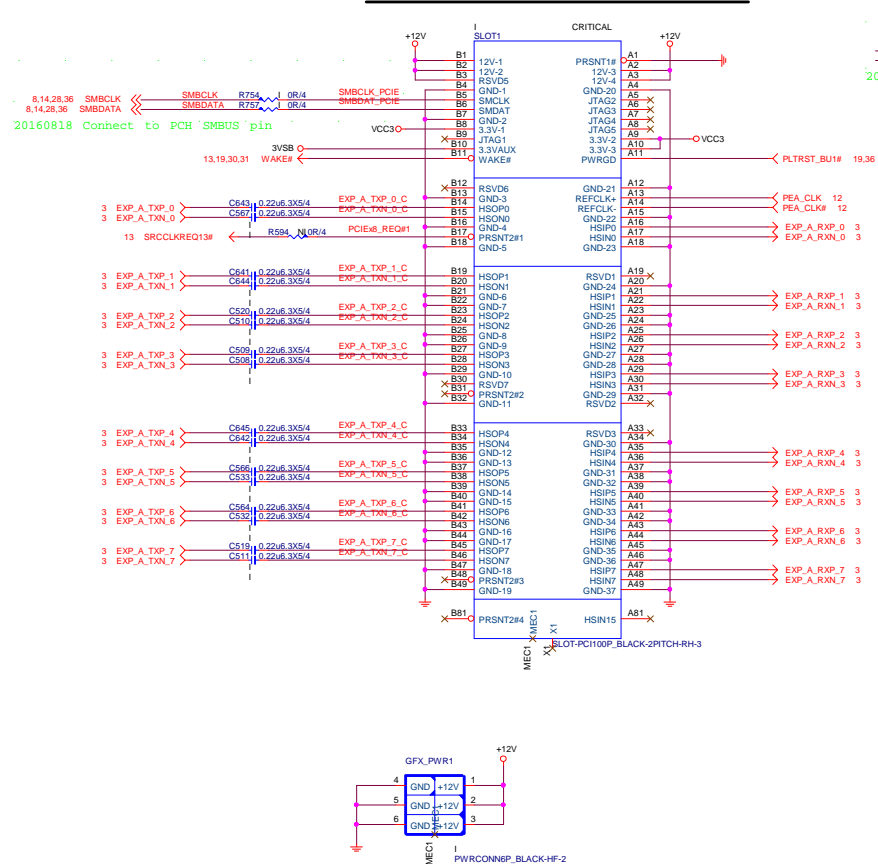
CLEAR CMOS DETECTION



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PCI_EXPRESS x16 SLOT2 (x8 Lanes)




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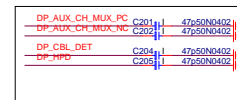
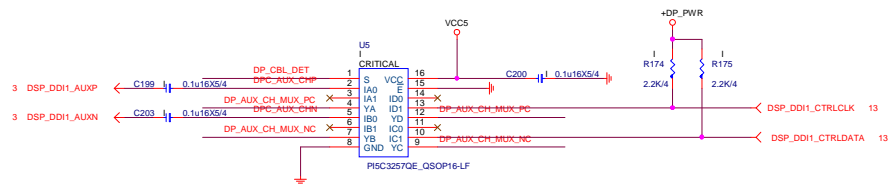
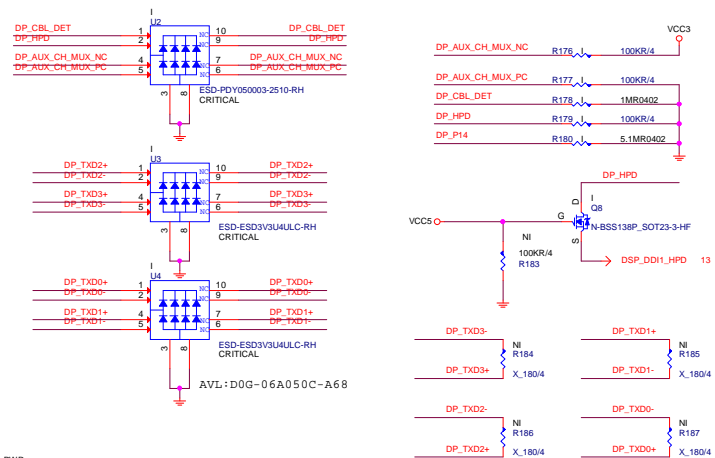
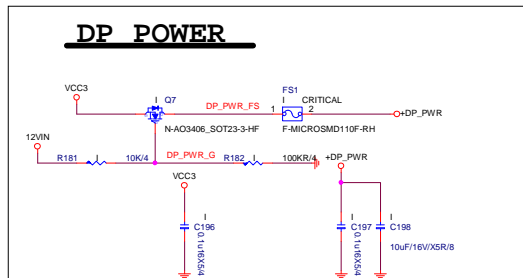
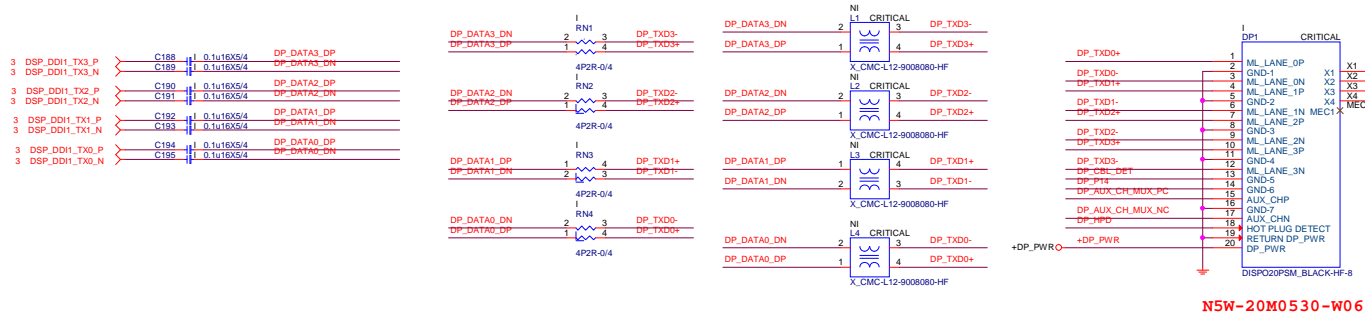


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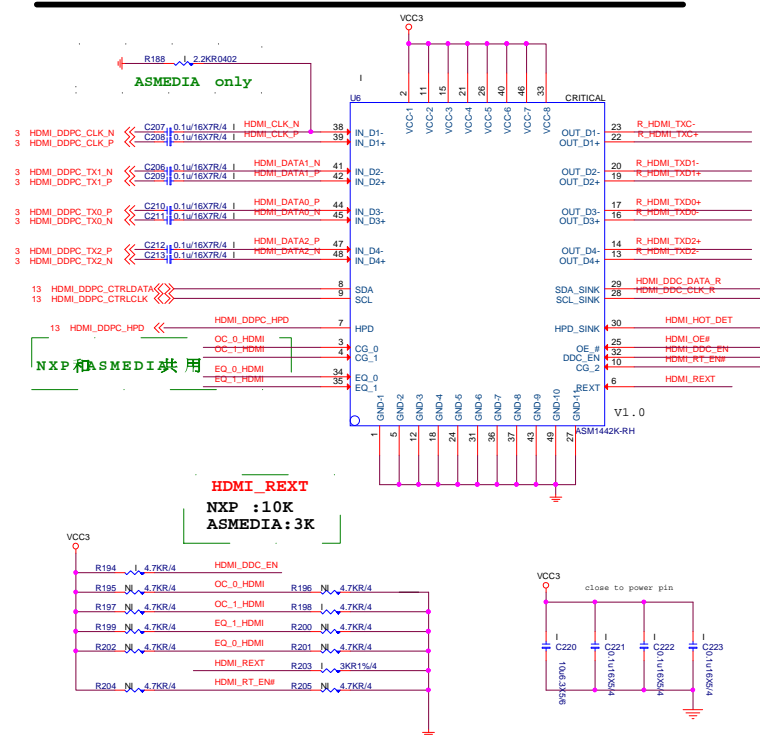
DP V1.2



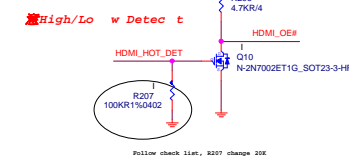
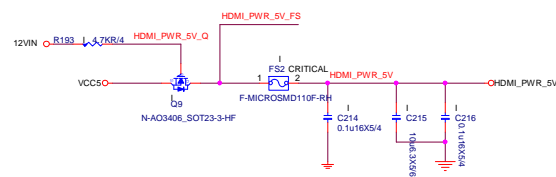
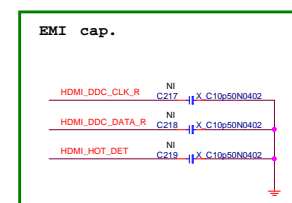
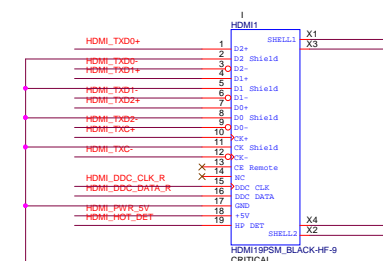
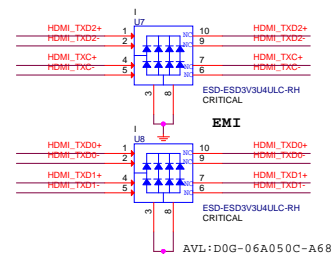
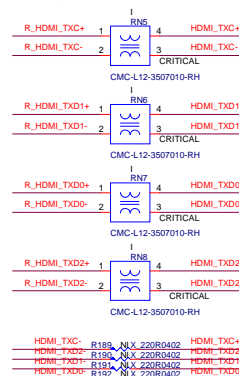
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AVL : B0B-033600C-N47 (NXP)



CM P/N: L12-6708010-I05



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NXP strapping set t i m g t a b l e

n.c.	4, 19, 34, 35	-	not connected
PG5	3	3.3 V low-voltage CMOS query input	Flasher setting input pin. This pin can be board-strapped to one of five decode values: short to GND, resistor to GND, open-circuit, resistor to V _{DD} , short to V _{DD} . See table 4 for truth table.

Equalizer

The PTN3360D supports 5 level equalization setting by the quinary input pin EQ5.

Inputs	Gainary notation	Equalizer mode
EQs		
short to GND	0s	0 dB
10 k Ω resistor to GND	1s	2 dB
open-circuit	2s	3.5 dB
10 k Ω resistor to V _{DD}	3s	9 dB
short to V _{DD}	4s	7 dB

ASMEDIA strapping set t i n g t a b l e

Strapping Table

TMD5 Input Signal Equalization

EQ_1	EQ_0	Equalization	Note
0	0	6dB	
0	1	2dB	
1	0	1dB	
1	1	0dB	

TMD5 Output Signal Integrity

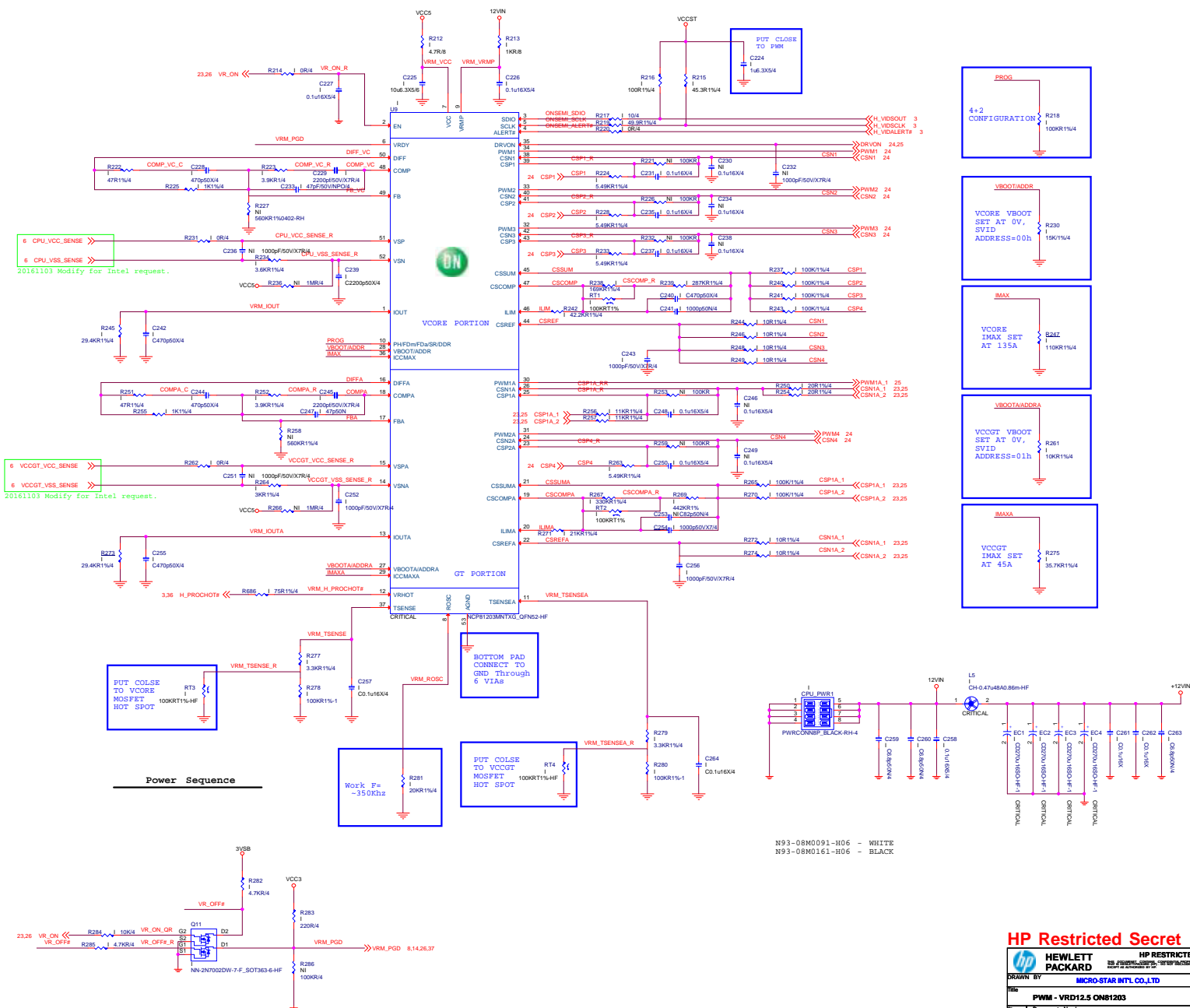
CC-0	CC-1	CC-0	Small	Pre-amp	Remains	Note
0	0	0	423	0	0	
0	0	1	458	0	-0.55dB	
0	1	0	461	0	-1.80dB	(info)
0	1	1	465	0	-0.36dB	
1	0	0	472	0	-1.60dB	
1	0	1	430	0.36dB	0	
1	1	0	422	0.36dB	0	
1	1	1	428	0	0	

SN	Model Name	Model Type	Model Size	Model Path
1	Model 1	Model 1	Model 1	Model 1
2	Model 2	Model 2	Model 2	Model 2
3	Model 3	Model 3	Model 3	Model 3
4	Model 4	Model 4	Model 4	Model 4
5	Model 5	Model 5	Model 5	Model 5
6	Model 6	Model 6	Model 6	Model 6
7	Model 7	Model 7	Model 7	Model 7
8	Model 8	Model 8	Model 8	Model 8
9	Model 9	Model 9	Model 9	Model 9
10	Model 10	Model 10	Model 10	Model 10

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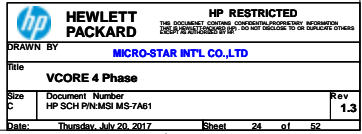
VOLTAGE REGULATOR MODULE (IMVP8)



N93-08M0091-H06 - WHITE
N93-08M0161-H06 - BLACK

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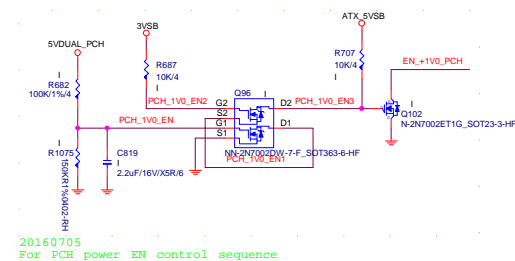
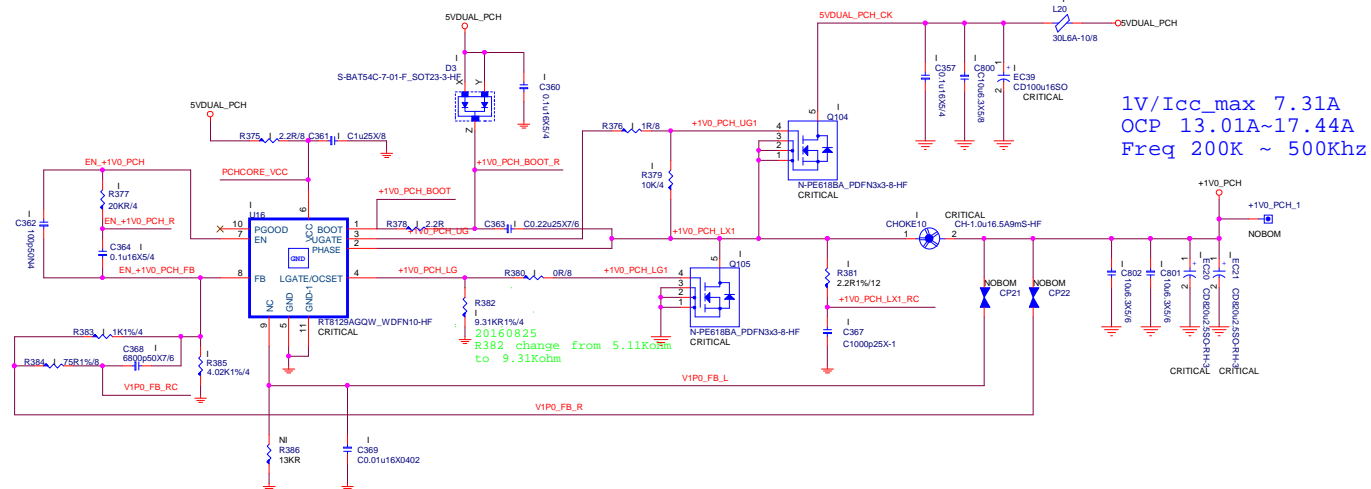
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					1.
Date:	Thursday, July 20, 2017	Sheet	23	of	52



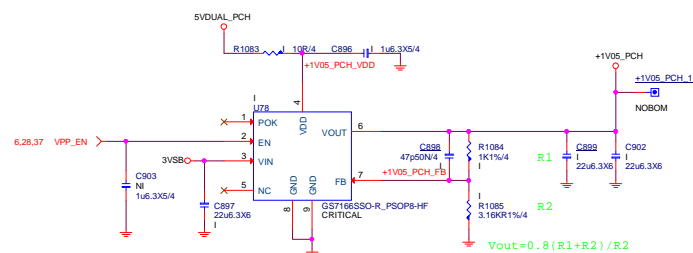


I32-8129A0C-R11
AVL : I32-1589L0C-O05

+1V0_PCH



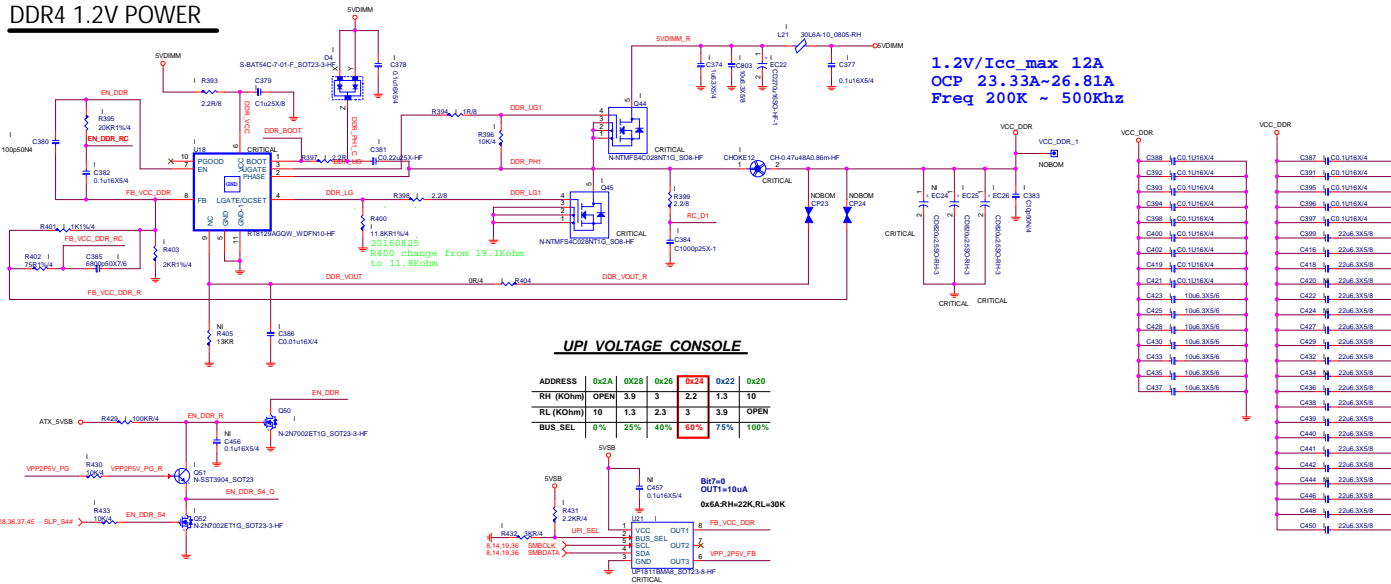
+1V5_PCH



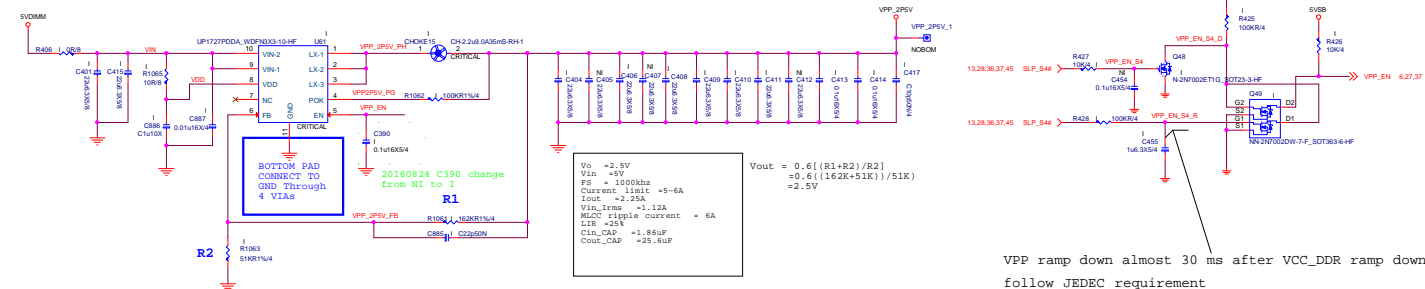
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Title <u> </u>			
PCH core power			
Size C	Document Number HP SCH PIN/MSI MS-7A61		Rev 1.
Date:	Thursday, July 20, 2017	Sheet 27	of 52

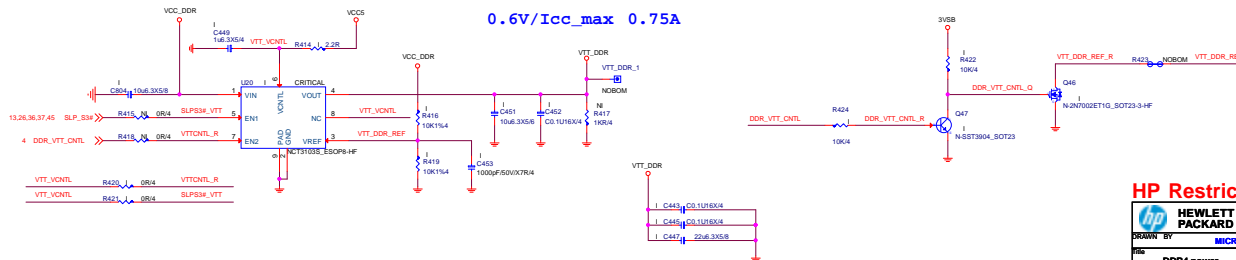
DDR4 1.2V POWER



DDR4 2.5V POWER



VTT DDR 0.6V Power



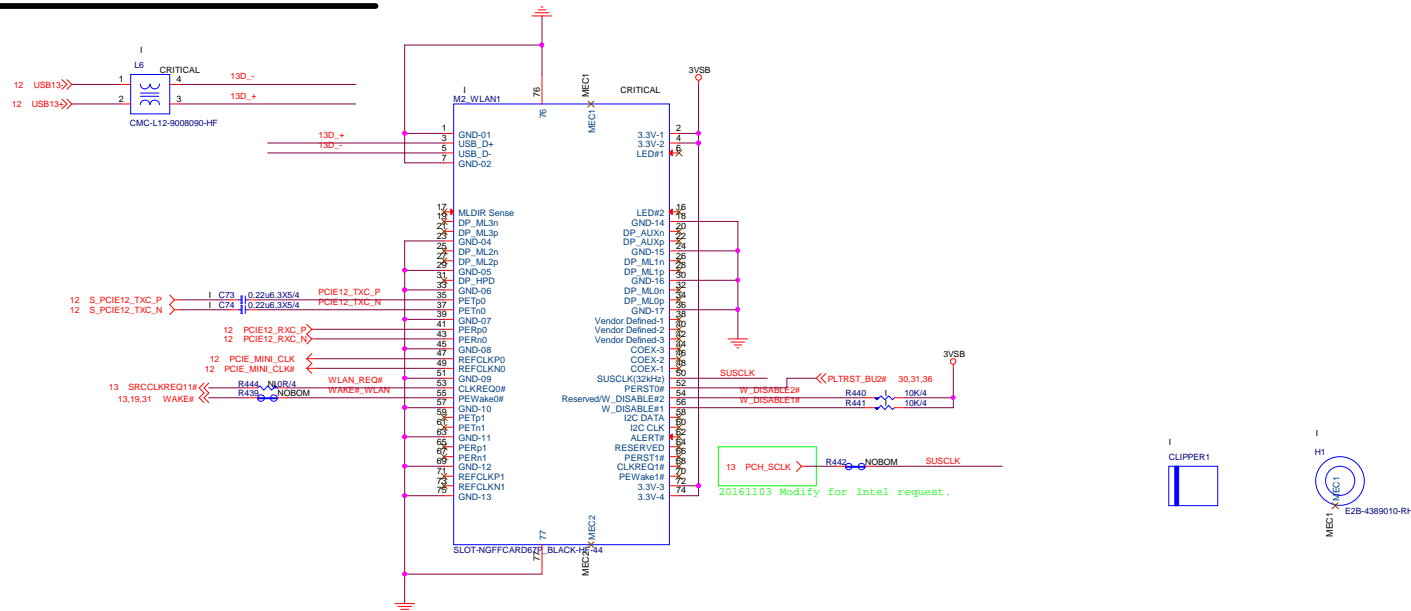
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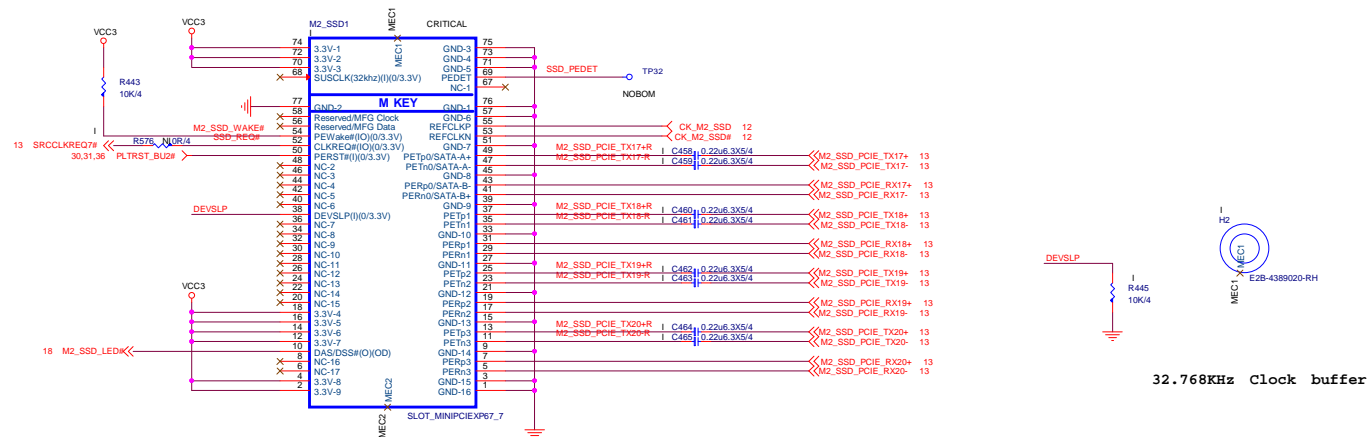
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Title	
Reserve	
Size C	Document Number HP SCH PIN:MSI-MS-7A61
Date: Thursday, July 20, 2017	Sheet 29 of 52
	Rev 1.

WLAN Key A plating GF & Height 8.5mm



M2 SSD-KEY-M

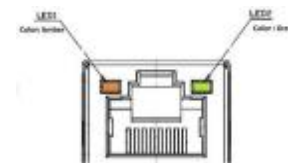
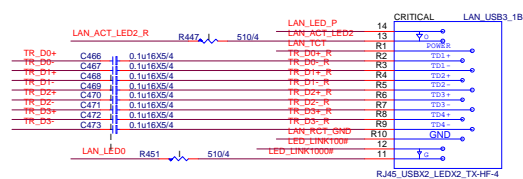
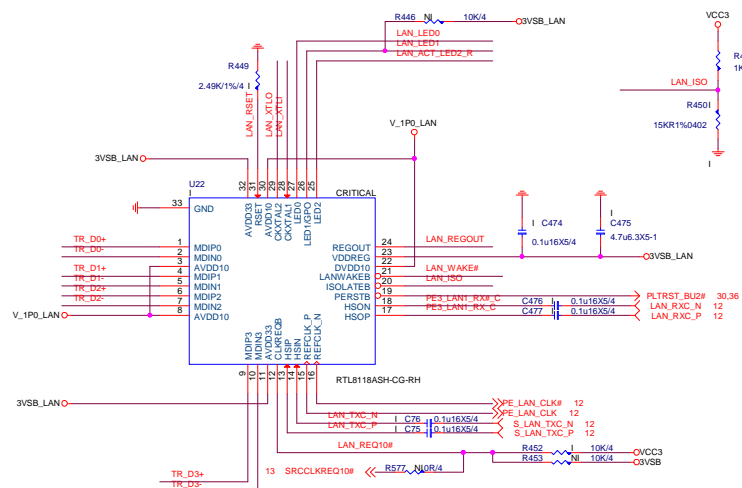


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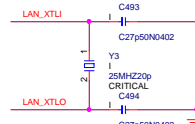
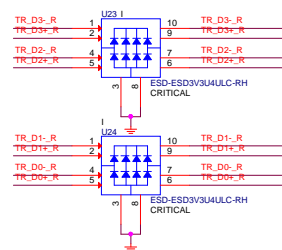
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Title: M.2 Slot - WLAN/SSD			
Size	Document Number	Rev	
C	HP SCH PIN/MSI MS-7A61	1.3	
Date:	Thursday, May 20, 2017	Sheet	30 of 52

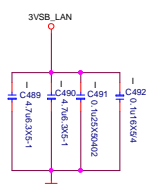
LAN Connector



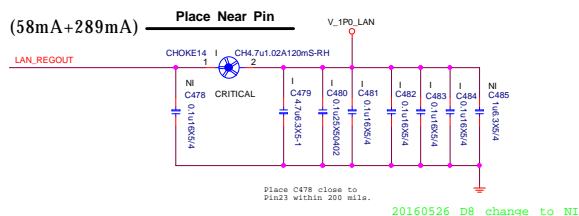
ESD



Place Near Pin

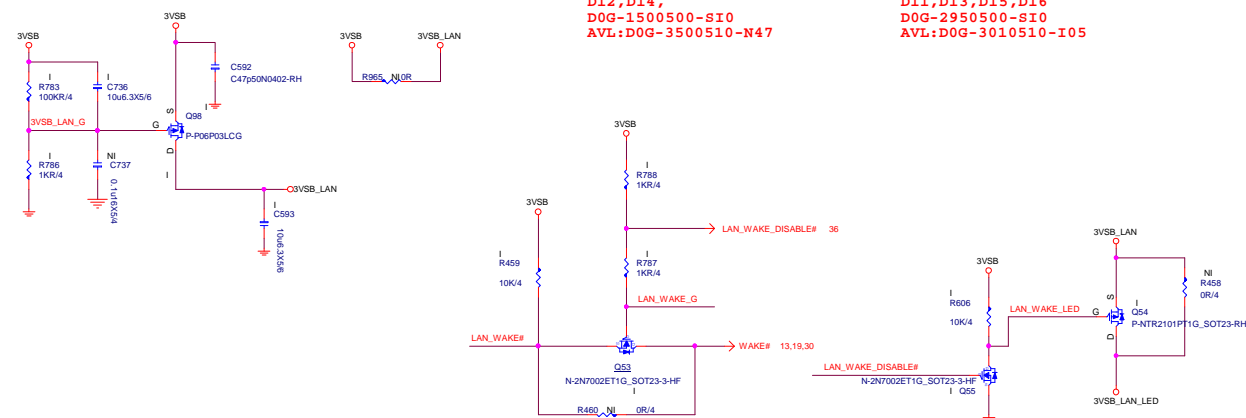


Place Near Pin



20160526 D8 change to NI

LAN Power stand by control

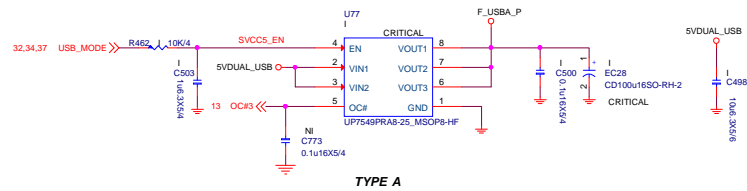


VCL ON	Speed	Active/Idle Mode		
		S3	S5/S4	S5
Active LED	J5 BR	1.1k	1.1k	None
	J5 GRN	4.7k	4.7k	Active
	J5k	1.1k	1.1k	None
	J5M BR	1.1k	1.1k	None
	J5M GRN	4.7k	4.7k	Active
Link Speed LED	J5 BR	4.7k	4.7k	None
	J5M GRN	1.1k	1.1k	1.5Gbps
	J5k	1.1k	1.1k	1.5Gbps
VCL OFF		S3	S5/S4	S5
Active LED	J5 BR	None	4.7k	None
	J5 GRN	None	4.7k	None
	J5k	None	4.7k	None
	J5M BR	None	4.7k	None
	J5M GRN	None	4.7k	None
Link Speed LED	J5 BR	None	4.7k	None
	J5M GRN	None	4.7k	None
	J5k	None	4.7k	None
Link Q.T		S3	S5/S4	S5
Active LED	J5 BR	4.7k	4.7k	None
	J5 GRN	4.7k	4.7k	None
	J5k	4.7k	4.7k	None
	J5M BR	4.7k	4.7k	None
	J5M GRN	4.7k	4.7k	None
Link Speed LED	J5 BR	4.7k	4.7k	None
	J5M GRN	4.7k	4.7k	None
	J5k	4.7k	4.7k	None

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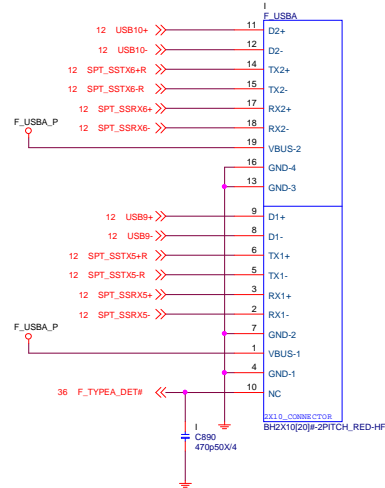
USB3.1 TYPE C / TYPE A



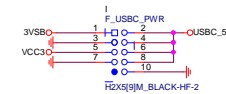
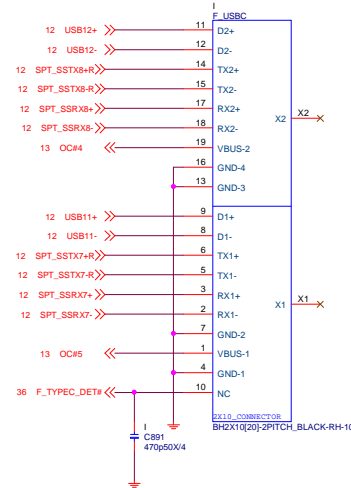
TYPE A

TYPE C

RED-90



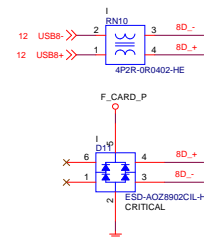
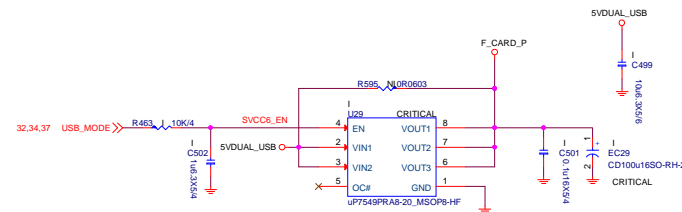
BLACK-180



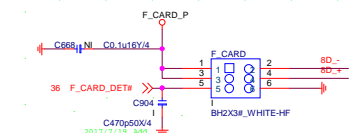
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TIO CARD Reader

placement close to 5VSB power rail at UP7550



N32-2030191-H06
BOX header / right angel

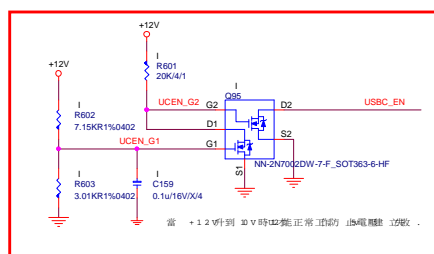
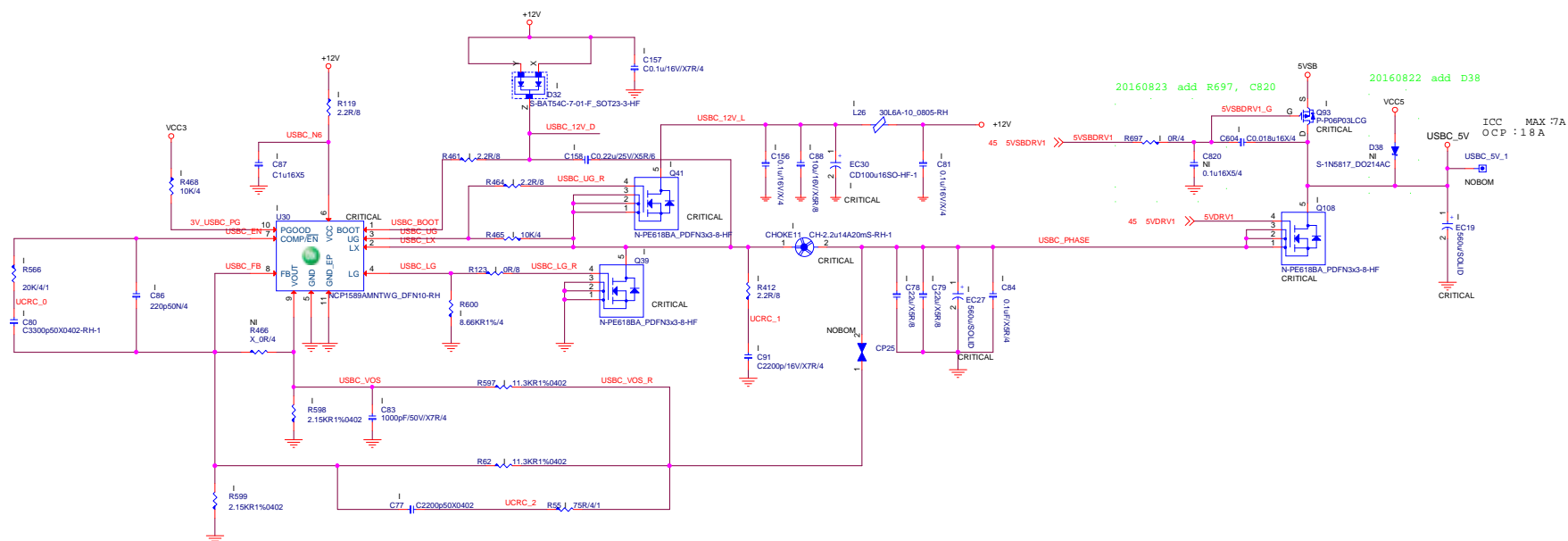


20160622
Connector change from N31-2031291-H06
to N32-2030191-H06 for ME team request

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Title		TIO USB3.0/Card header	
Size	Document Number	Rev	
C	HP SCH PIN/MSI MS-7A81	1.3	
Date:	Thursday, May 20, 2017	Sheet	32 of 52

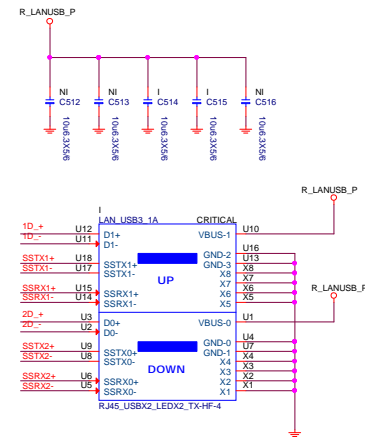
TIO USB TypeC power



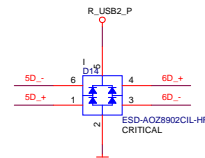
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Title TIO USB TypeC power			
Size C	Document HP SCH PIN:MSI MS-7A61		Rev 1.
Date:	Thursday, July 20, 2017	Sheet 33	of 52

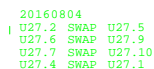
Rear USB3.0 + LAN



Rear USB2.0




Rear USB3.0



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Title Rear USB3.0/RJ45		
Size C	Document Number HP SCH PIN3MSI MS-7A61	Revision 1
Date: Tue, July 20, 2017		
Sheet 34 of 52		

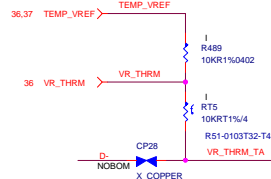
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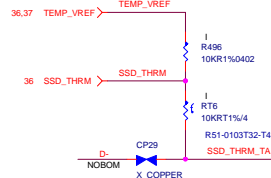
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Title		Reserve			
Size	Document Number	Rev			
C	HP SCH PINMSI MS-7A81	1.3			
Date:	Thursday, July 20, 2017	Sheet	35	of	52

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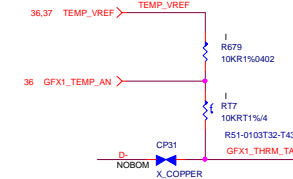
Place close to VRM MOSFET Thermistor



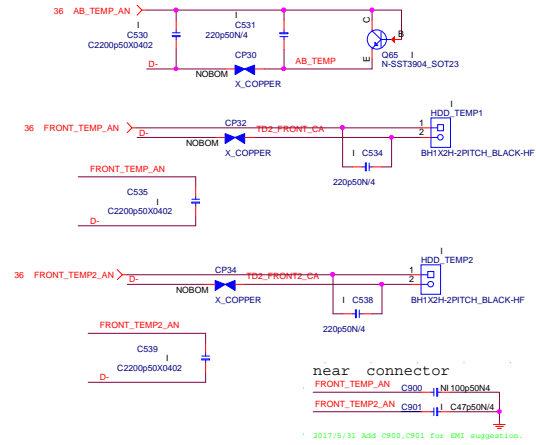
Place close to M.2 SSD slot Thermistor



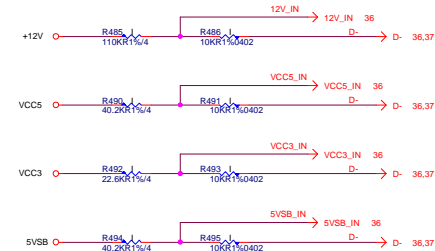
Place close to GTX slot Thermistor



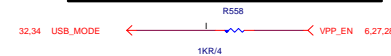
Thermal diode Sensor



HW monitor



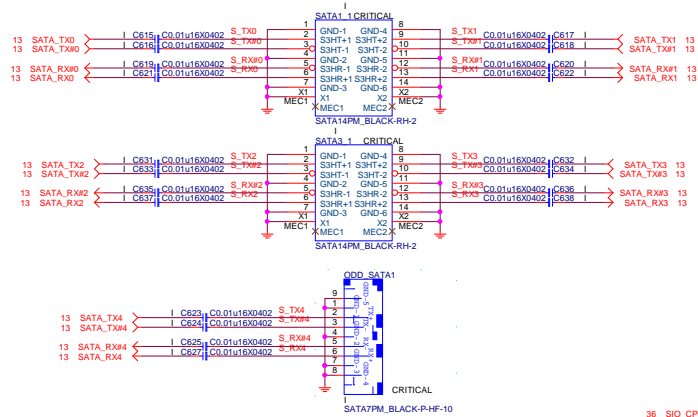
USB power support S0/S3



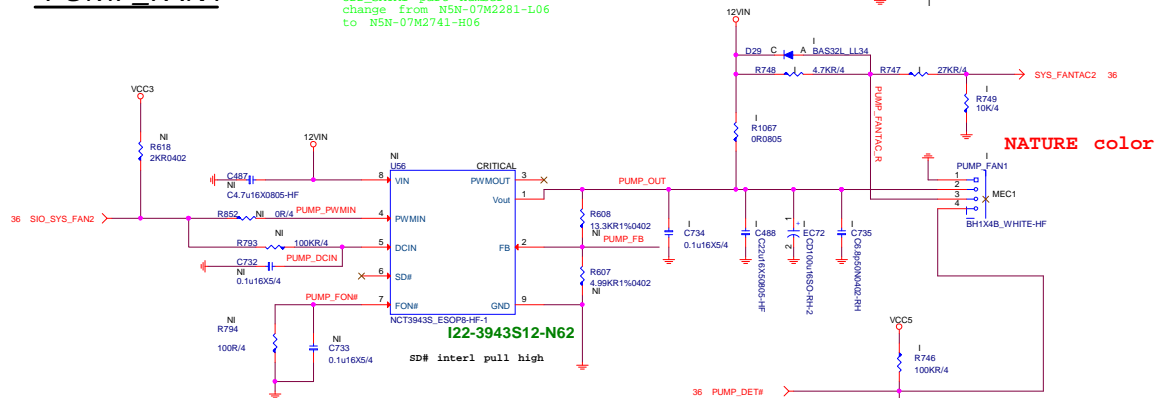
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Title		SIO NCT6683 D-T II	
Size		Document Number	
C		HP SCH PANMSI MS-7A61	
Date:		Thursday, May 20, 2017	Sheet 37 of 52

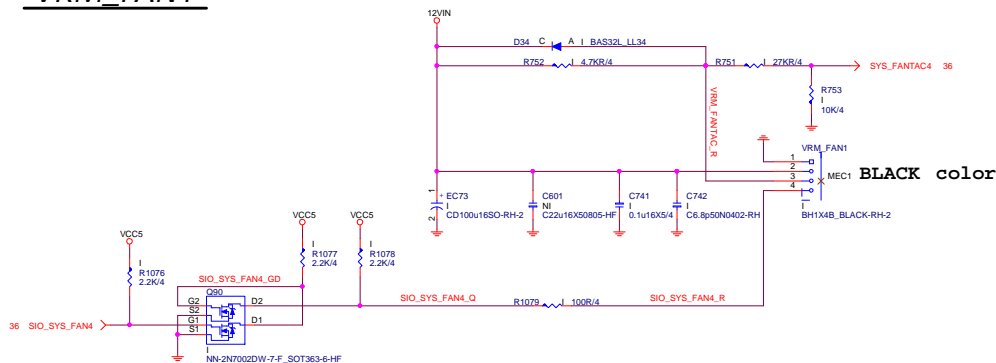
SATA port



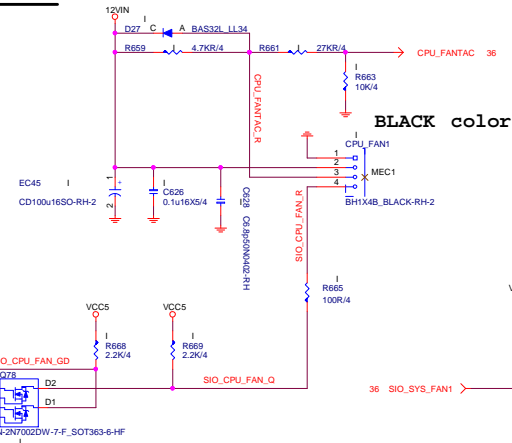
PUMP_FAN1



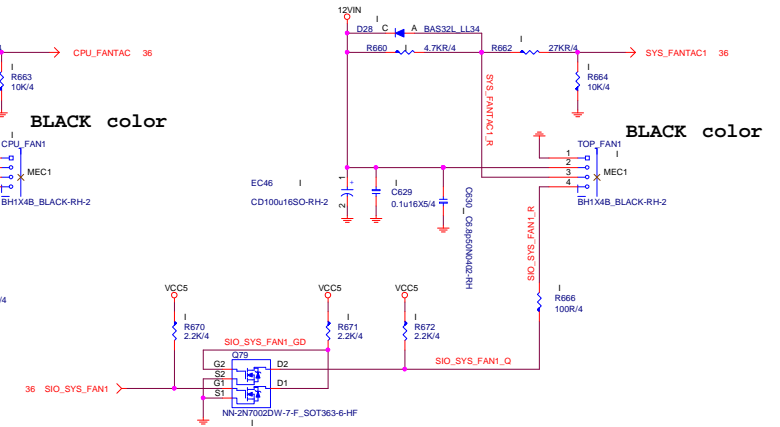
VRM_FAN1



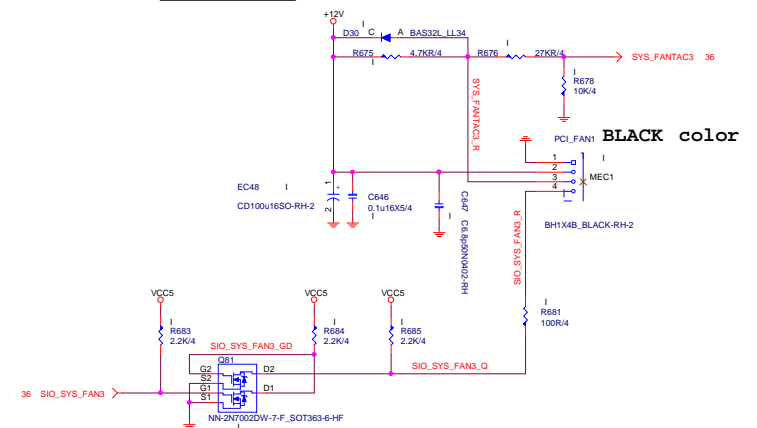
CPU_FAN1



REAR_FAN1



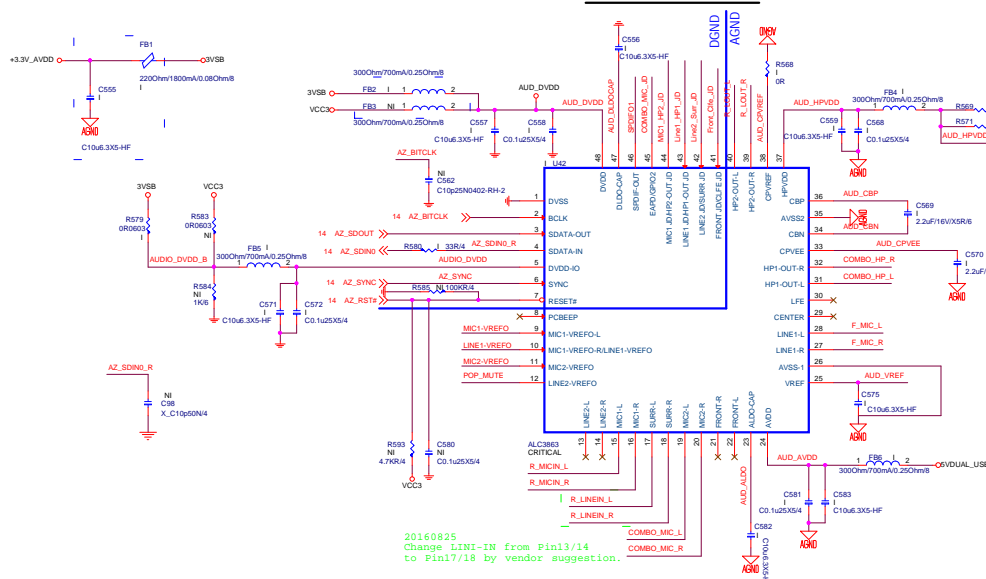
PCI_FAN1



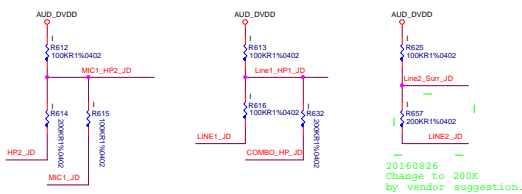
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Title SATA / FAN Control					
Size	Document Number				Rev
Custom	HP SCH P/N:M51 MS-7A61				1.3
Date: Thursday, July 20, 2017		Sheet 36		of 52	

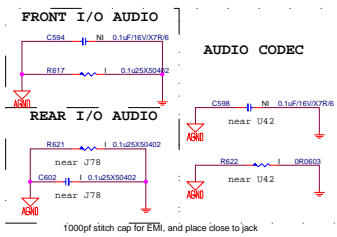
ALC-3863 circuit



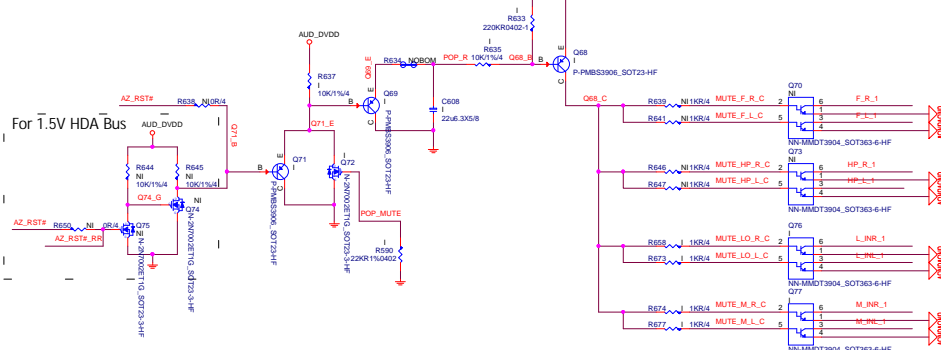
Sense circuit



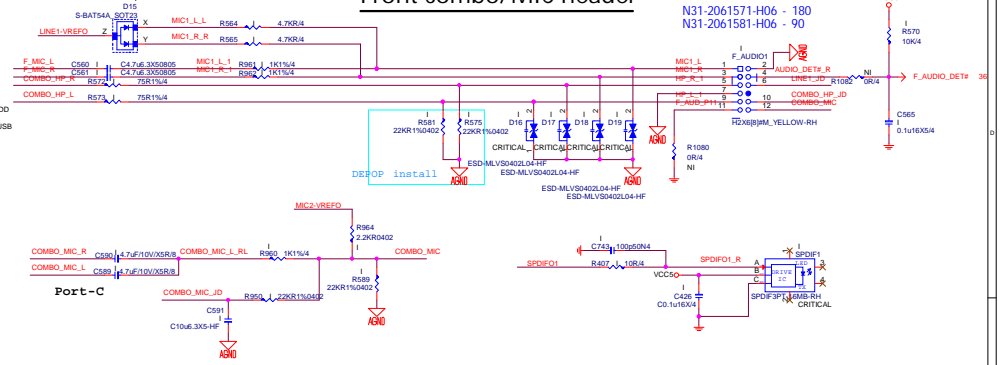
EMI Solution



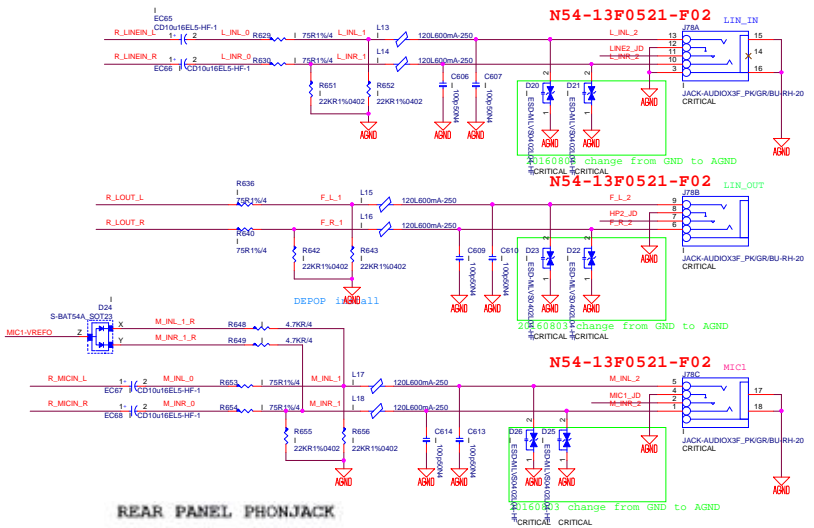
DE-POP circuit



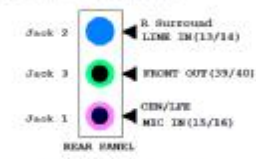
Front combo/MIC header



Rear Phone Jack 3 IN 1



REAR PANEL PHONJACK



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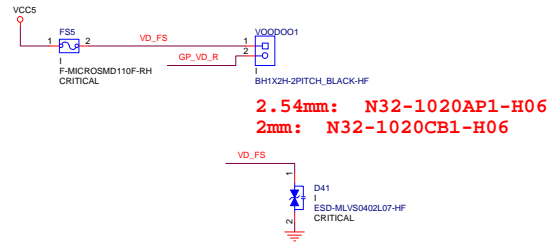
ALC3863 Configuration (5.1 Channel)

Pin	Signal	Location	Function
1	HP1 (pin=1,4)/Port=1	Front Panel	Front Out
2	LINE1 (pin=1,4)/Port=2	Front Panel	Line In
3	MIC1 (pin=2,3,4)/Port=3	Front Panel	COM/LFE, Mic In
4	HP2 (pin=5,6)/Port=4	Front Panel	Front Out
5	MIC2 (pin=5,6)/Port=5	Front Panel	COM/LFE, Mic In
6	HP3 (pin=7,8)/Port=6	Front Panel	Front Out
7	MIC3 (pin=7,8)/Port=7	Front Panel	COM/LFE, Mic In

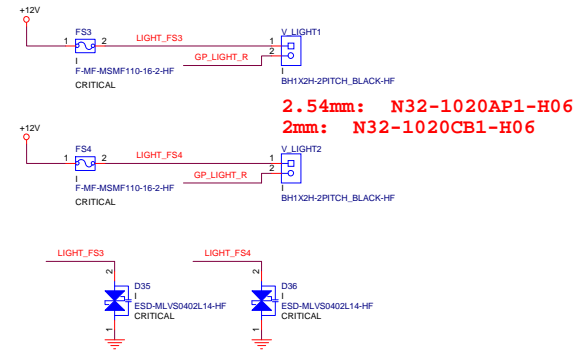
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Model	Audio Codec ALC3863	
Size	Document Number	Rev
HP	HP SCH PAK MS 7461	1.3
Date	Thursday, 28/05/2017	Sheet 39 of 52

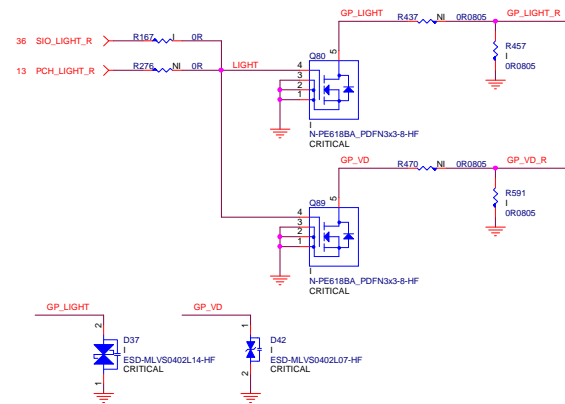
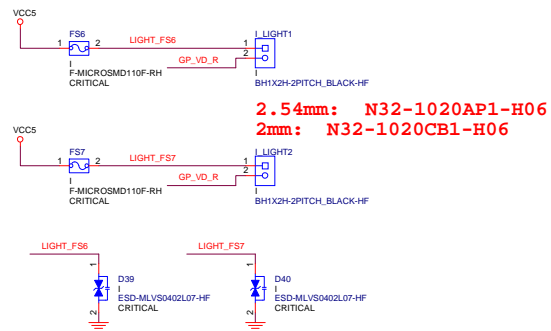
VOODOO logo lighting



V bar lighting



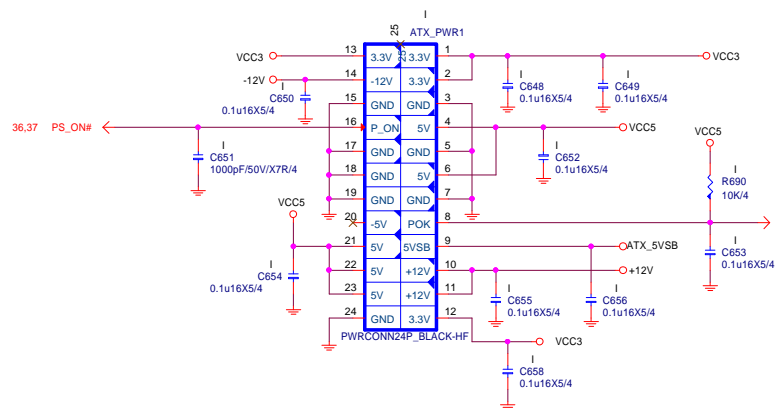
Internal lighting



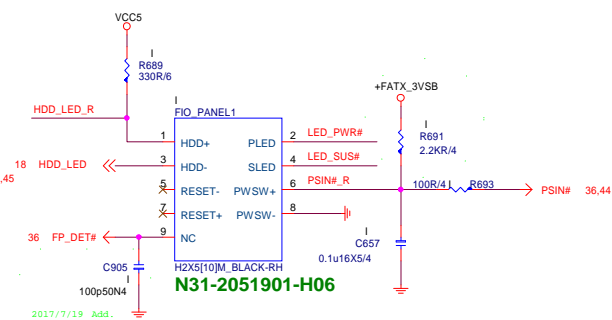
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Title		LED lighting	
Size	Document Number	Rev	
C	HP SCH PIN/MSI MS-7A81	1.3	
Date:	Thursday, July 20, 2017	Sheet	40 of 52

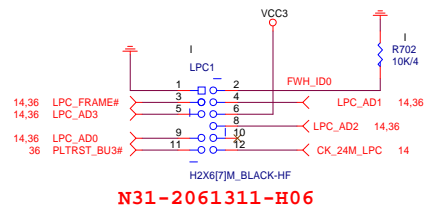
ATX 24pin header



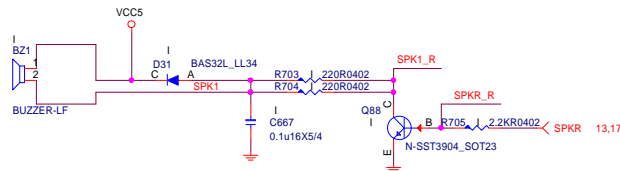
Front Panel



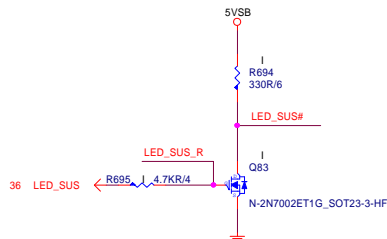
LPC Debug Port



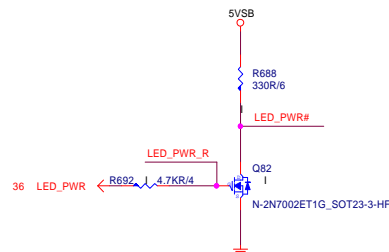
Internal Buzzer



SUS LED



Power LED



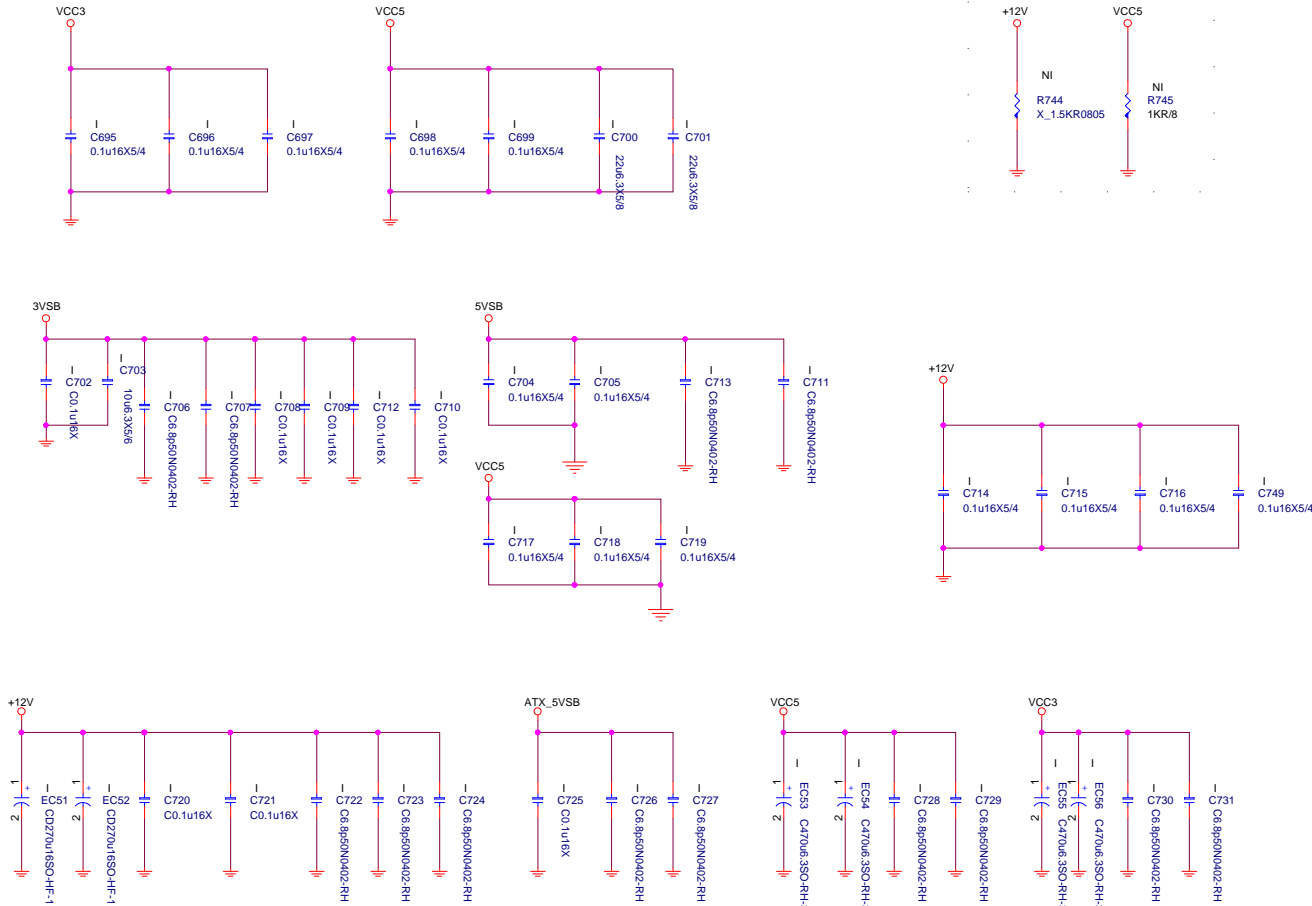
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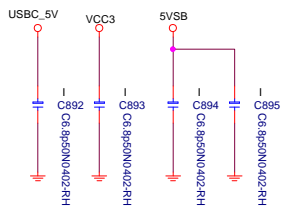
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Title		F_Panel/Buzzer/Debug/ATX24			
Size	Custom	Document Number	HP SCH P/N-MSI MS-7A61	Rev	1.3
Date:	Thursday, July 20, 2017	Sheet	41	of	52

EMI Decoupling Cap

discharge patch resistor



RFI Decoupling Cap

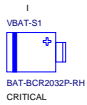


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Title EMI solution			
Size	Document	Number	Rev
Custom			1.3
Date: Thursday, July 20, 2017		Sheet 42 of 52	



P80-07A6113-E48
AVL:P80-07A6113-G37



E22-B009010-C22
AVL:E93-0000099-A21



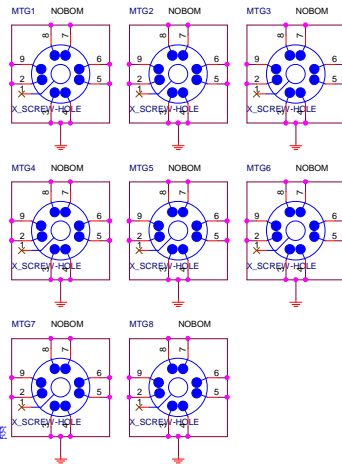
E21-AC71010-L06
AVL:E21-7826010-F02

E22-B009010-C22 - HP CPU 條
AVL:E93-0000099-A21

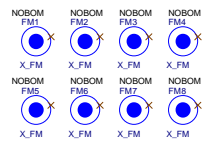
E21-AC71010-L06 - HP 底座
AVL:E21-7826010-F02

E21-7869020-F02 - Channel CPU 條
E93-0000100-H06 - Channel 底座

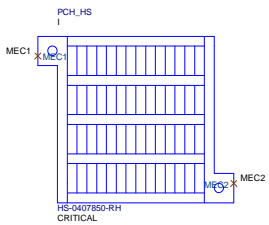
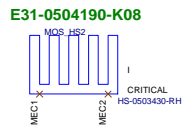
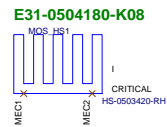
Mounting Holes



Optical Fiducial Marks-X

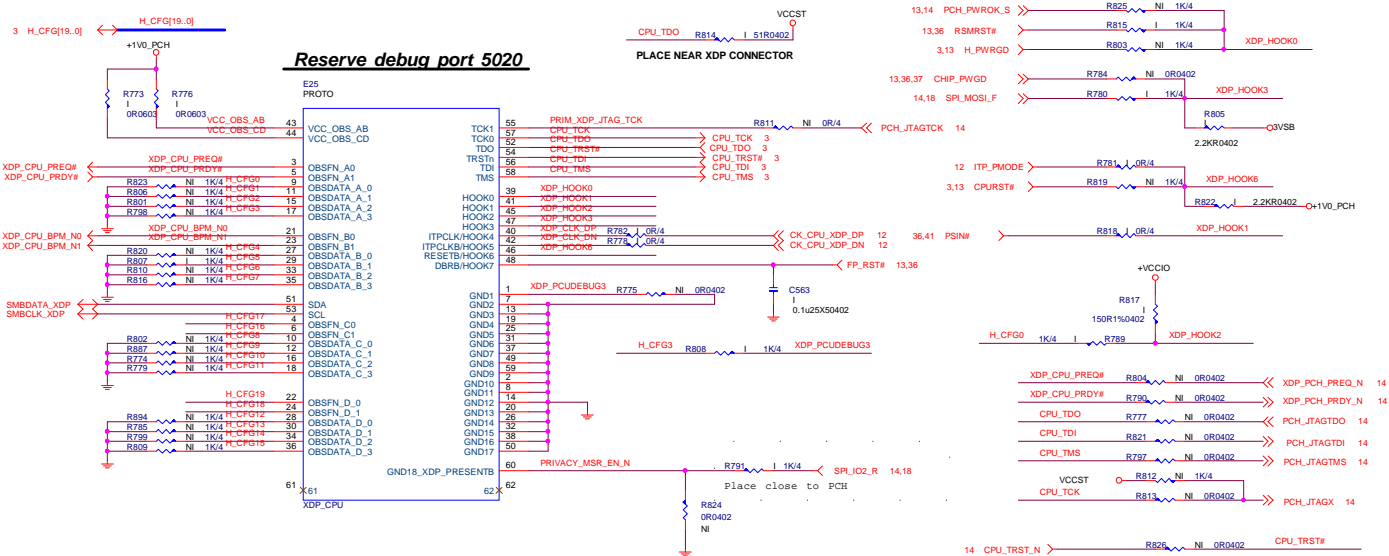


Simulation

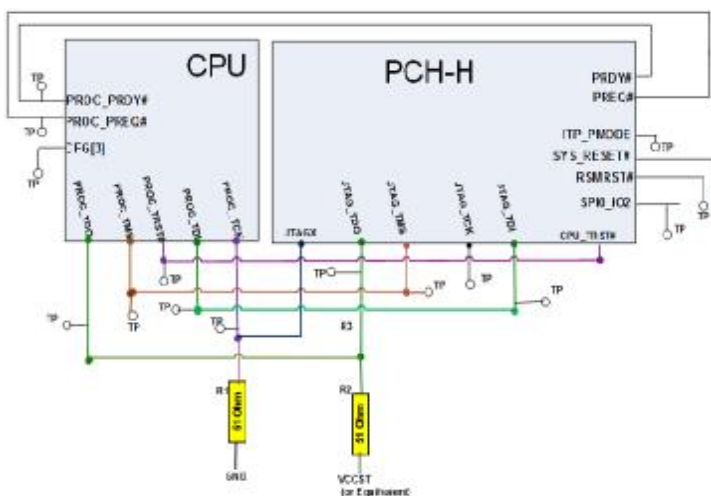


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DCI Connect



For DCI Support

R804(0 ohm)/R790(0 ohm)/R777(0 ohm):I
R821(0 ohm)/R797(0 ohm)/R813(0 ohm)/R826(0 ohm):I
R814 (51 ohm): NI
R829(51 ohm)/R831(51 ohm):NI (Page 14)
R52 (51 ohm):NI (Page 3)

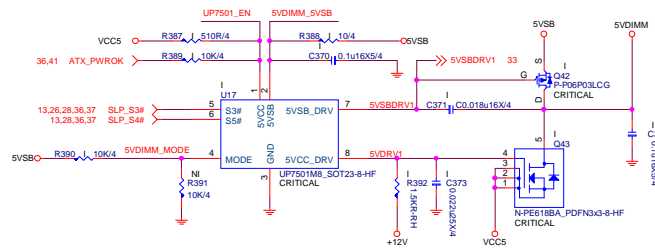
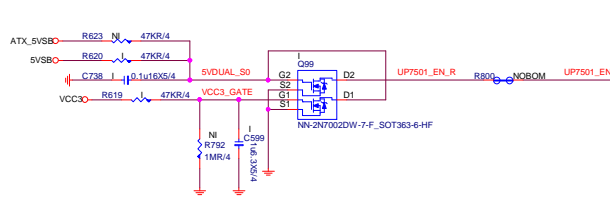
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> CFG[0]: Stall reset sequence after PCH R1 lock until de-asserted. <ul style="list-style-type: none"> 1 = (Default) Normal Operation No stall. 0 = Stall. CFG[1]: Reserved configuration lane. CFG[2]: PCI Express® Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. CFG[3]: eDP® enable. <ul style="list-style-type: none"> 1 = Disabled. 0 = Enabled. CFG[6:5]: PCI Express® Bifurcation <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express® 01 = reserved 10 = 2 x8 PCI Express® 11 = 1 x16 PCI Express® CFG[7]: PEG Training. <ul style="list-style-type: none"> 1 = (default) PEG Train immediately following RESET# de-assertion. 0 = PEG Wait for BIOS for training. CFG[19:6]: Reserved configuration lanes. 	I	5VTL	dc	All processor lanes. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.

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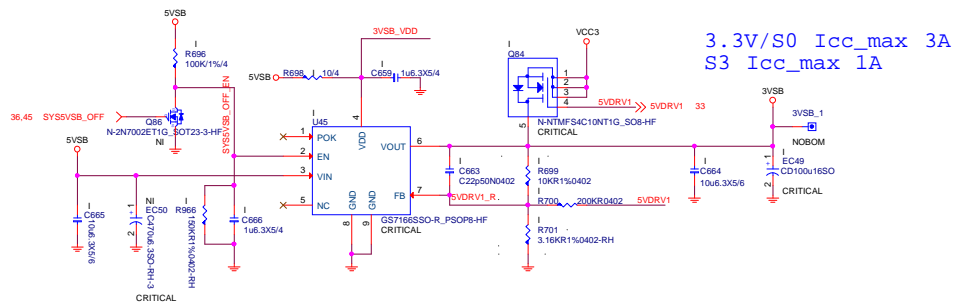
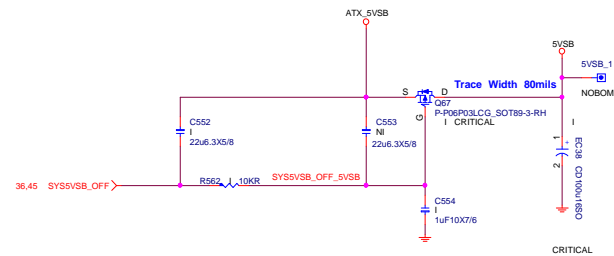
5VDIMM Power Switch

S0,S3,S4,S5 5VDIMM power rail working.
only Deep S5 no power.



5VSB Power Switch

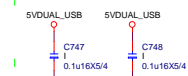
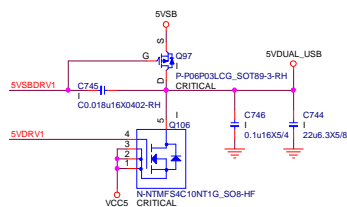
3VSB Power Rail



3.3V/S0 Icc_max 3A
S3 Icc_max 1A

5VDUAL_USB Power Switch

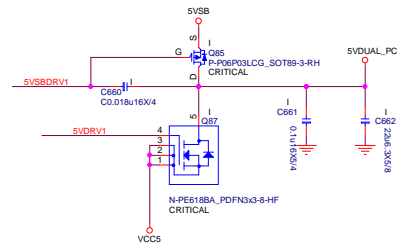
Stitching Cap



20160817 Add stitching cap for cross moat signal

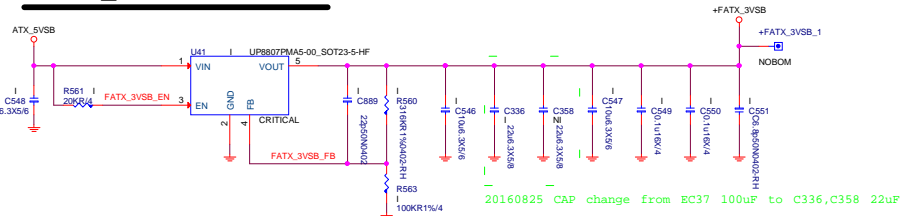
5VDUAL_PCH Power Switch

S0,S3,S4,S5 5VDUAL_PCH power rail exist.
only Deep S5 no power.



+FATX_3VSB Power Rail

I_max 0.21A

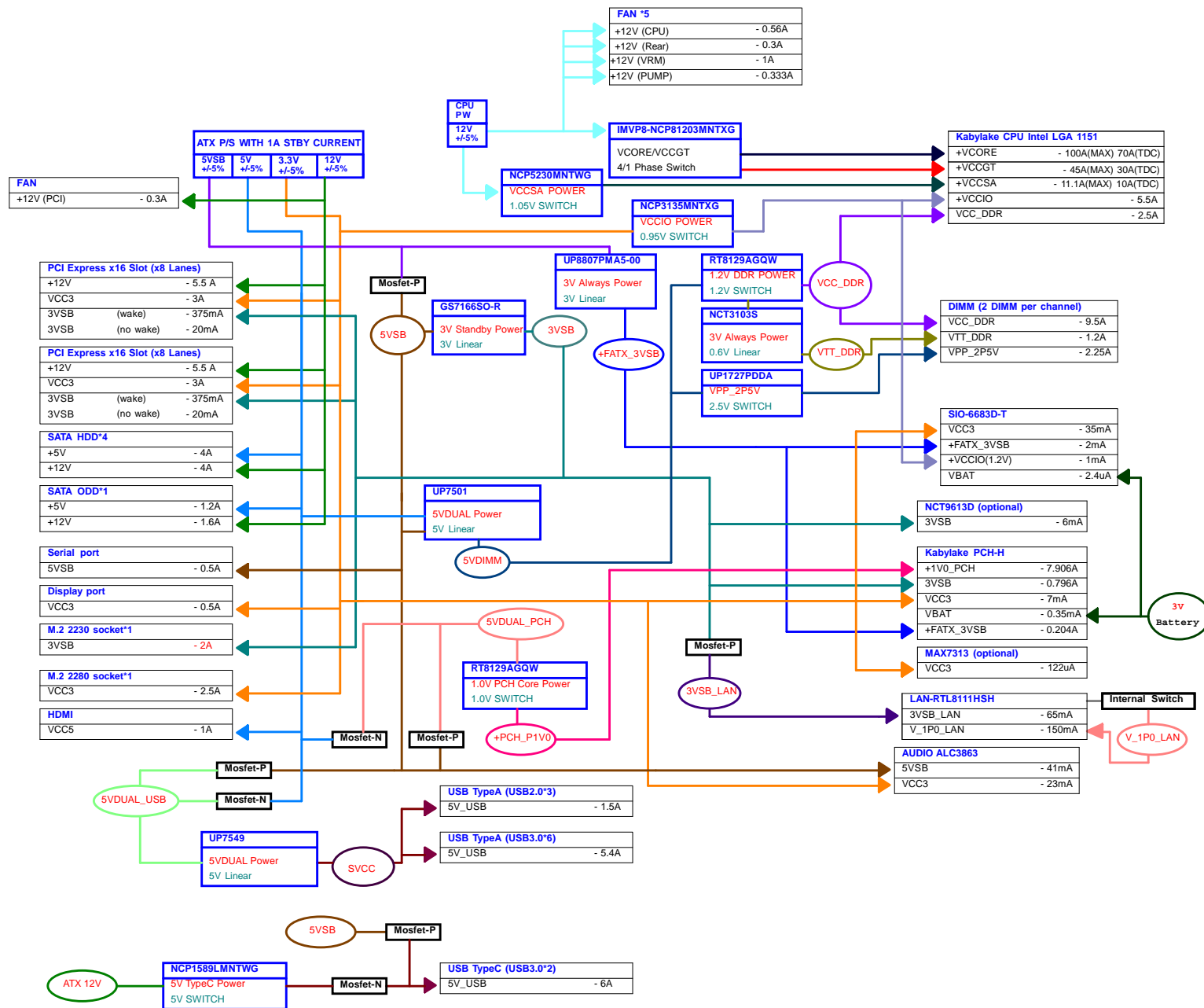


20160825 CAP change from EC37 100uF to C336,C358 22uF

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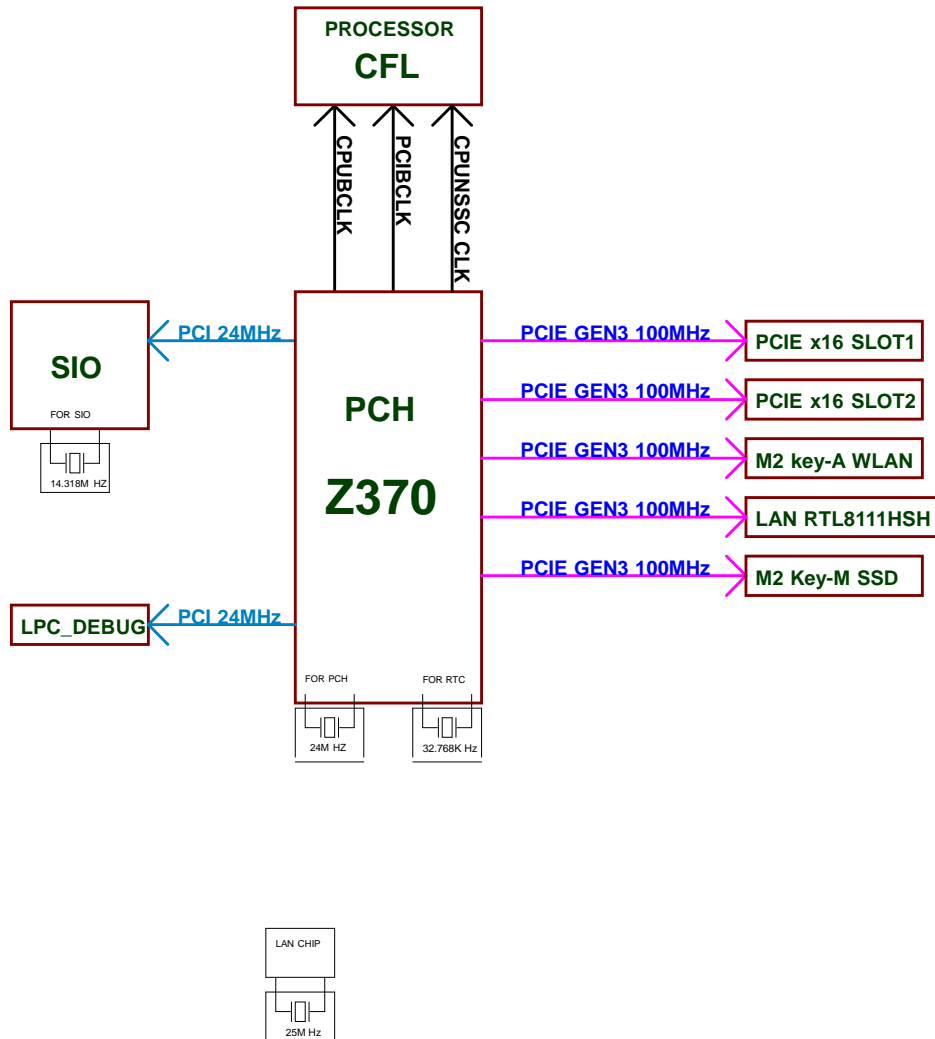
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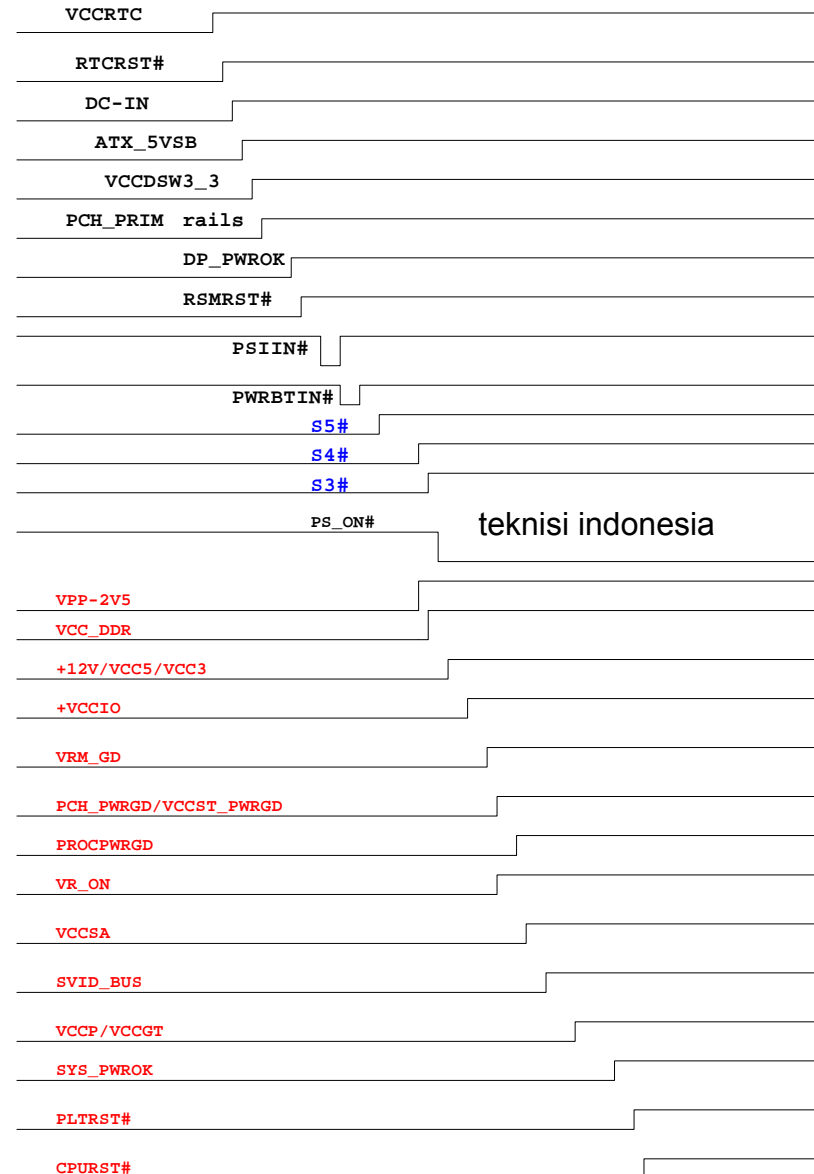
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CLK MAP



Power ON Sequence

G3-->S5-->S0



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Kabylake PCH-H Z370

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NCT 6683 D-T

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DDR-4 DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	000	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 2	001	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 3	010	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1
DIMM 4	011	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3

Power On Strapping Table form NCT6683 D-T

Symbol	Value	Description
2E_4E_SEL	0	SIO I/O address is 2Eh/2Fh
	1	SIO I/O address is 4Eh/4Fh
BKFD_EN	0	Pin67 3VSB# SW#, Pin69 RSTOUT0#
	1	Pin67 BKFD_CUT, Pin69 LATCHED_BKFD_CUT
TESTMODE1	0	Please always pull down this pin with 1Kohm resistor.
	0	Hardware ACPI could take over related signals
DIS_HWACPI	1	Hardware ACPI never take over related signals
		Output "0": Pin68 10# 12# 124
		Output "1": Pin68 10# 12# 124
TESTMODE2 (SPI_CS#_SIO)	0	Configuration Register I/O port is 4E/4F.
SBI_CFG_EN (SPI_CLK_SIO)	0	Switches open or close are determined by ATXPGD
	1	Switches open or close are determined by configuration register



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0B

2016/10/11

Page 26: Rename net VCCSA_COMP C to VCCSA_COMP.
Page 14/36: Modify SUS_WARN#/SUS_ACK# circuit.
R110/R111/R481/R497 change to NI, add R1072.
Page 13: Modify RSMRSTW circuit.
Add R1073/R1074/C888/Q110/Q111.
Page 45: Modify 3VSB circuit.
Modify R696 to 100Kohm, R966 to 150Kohm and I, Q86 to NI, EC49 to 100uF.
Page 27: Modify +LV0_PCH control circuit.
Modify C819 to 1uF, add R1075.
Page 23: Modify VRM control circuit.
Modify R214 to 0ohm, modify R346 to 4.7Kohm.
Page 34: Modify R_USB2_P power circuit.
Rename SVCC3_EN to SVCC2_EN, modify C639 to 0.22uF.
Page 13: Fix 3VSB has leakage.
Modify R72 to NI.
Page 36: Modify DPMWOK circuit.
Modify R1069 to 1.47Kohm.

2016/10/13

Page 38: Modify VRM_FAN1 circuit.
Delete R624, C600, R853, R795, C739, R796, C740, R631, R626.
Modify C601 to NI, EC73 to I.
Change VRM_FAN1 part number to N32-1040CF1-H06.
Add Q90, R1076, R1077, R1078, R1079.

2016/10/14

Page 23: Modify VRM circuit.
Modify R234 from 3.3K to 3.6K, R245 from 30K to 29.4K, R273 from 30.1K to 28.7K,
C253 from 150pf to 82pf, C240 from 560pf to 220pf.
Page 23: Modify RT1,RT2,RT3,RT4 package from 0603 to 0402.
Page 22: Modify HDMI circuit.
Modify R205 from I to NI, R197 from I to NI, R198 from NI to I, R196 from I to NI.

2016/10/17

Page 23: Modify VRM circuit.
Modify R266 to NI.

2016/10/18

Page 40: Modify LED lighting circuit.
Add internal lighting circuit.

2016/10/19

Page 27: Modify +LV0_PCH control circuit.
Modify C819 to 2.2uF 0603
Page 26: Modify VCCSA power circuit.
Modify R363 from 9.53K to 8.66K, C389/C403 from 22uf/NI to 47uf/I,
CHOKE8 to L04-05A7321-L65.
Page 33: Modify USB_C5V power circuit.
Modify R600 from 11.8K to 8.66K.
Page 45: Modify 5VSB circuit.
Modify C552 from NI to I, C553 from I to NI, C554 from 0.1uf to 1uf,
EC38 from 470uf to 100uf, EC50 from I to NI.

2016/10/20

Page 26: Modify VCCSA power circuit.
R368 from 24K/NI to 9.09K/I.
Page 39: Modify Audio Codec ALC3863 circuit.
Modify F_AUDIO1 pin 11 from NC to GND.

2016/10/24

Page 15: Modify C162 from NI to I.
Page 13: Modify WAKE# pull-up power well from 3VSB to +FATX_3VSB.
Page 45: Modify +FATX_3VSB power circuit.
Modify R560 from 10K to 316K, R563 from 3.16K to 100K and add C889.

2016/10/25

Page 14: Modify LFC_DRQ#0/SERIRQ/KBRST#/TPM_CLKRUN# pull-up power well from 3VSB to VCC3.

2016/10/31

Page 32: Add 22pF cap at front USB detected pin.
Add C890,C891

2016/11/02

Page 36: Modify Y4 from DIP to SMD type, add R1081.
Page 39: Modify R642/R643 from NI to I.

2016/11/03

Page 42: Add C892, C893, C894, C895 6.8pF Cap for RFI

2016/11/18

Page 36: Modify PCB revision for SI.
Modify R552,R545 from I to NI, modify R553,R543 from NI to I.

0C

2017/01/18

Page 9/11: Modify DIMM slot color from Blue to Red.
DIMM2/DIMM4 from N13-2880981-L06 to N13-2881021-L06.
Page 41: Modify ATX 24 Pin connector color from White to Black.
ATX_PWR1 from N93-24M0201-H06 to N93-24M0321-H06.
Page 36: Modify Board revision ID to 0011.
Modify R553 from I to NI, R545 from NI to I.

Page 12: 32.768KHz crystal matching
Modify C82 and C90 from 15pf to 18pf.

Page 26: Modify VCCSA power circuit for power quality.
Modify R363 from 8.66K to 9.76K, modify C347,C349,C351,C352 from 22uf to 47uf.

Page 36: 14.318MHz crystal matching
Modify C536 and C537 from 24pf to 33pf.

0D

2017/03/02


Page 32: Modify C891,C890 from 22pf to 470pf.
Page 32: Modify F_USBC PN to N32-2101681-H06.

10

2017/03/20

Page 12-19: Modify PCH PN to MP PN.
PCH1 from OB1-7A61001-IX6 to B01-8222715-IX6.
Page 36: Modify Board revision ID to 0100.
Modify R543,R545,R551 from I to NI, R541,R552,R553 from NI to I.

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Hurricane 1.1

7A61-1.1 (SI)

2017/05/24
Page 03/04/05/06/07: Change CPU1 from skylake for coffee lake.
Page 6: Change R29.1 connection to +1V5_PCH.
Change R29 from NI to I.
Change Q1 from I to NI.
Page 27: Add U78,C896,C897,C898,C899,R1083,R1084,R1085,+1V5_PCH_1 for PCH 1.05V power.

2017/05/26
Page 6: Delete R732,R738,R741,R750.

2017/05/31
Page 23: Change C240 from 220pF to 390pF.
Change R247 from 107KR to 110KR.
Page 26: Change U14 from I9C-3135M0C-005 to I9C-3136M0C-005.
Page 37: Add C900,C901 for EMI suggestion.

2017/06/01
Page 27: Add C902,C903.
Change C899 from 0805 to 0603.
Change C898 from 560pF to 47pF.

2017/06/05
Page 3: Add TP48.

2017/06/07
Page 18: Add R1086.Change Q5 from I to NI.
Change U1 ASM from 5010 to 60.

2017/06/08
Page 18: Change U1 from M31-25Q6443-W03 to M31-2512893-W03.

2017/06/09
Page 36 Change Board ID
Change R541,R552 from I to NI.
Change R543,R551 from NI to I.


7A61-1.3 (PV)

2017/07/17
Page 6: Change C5 from 10u to 0.1u.
Page 23: Change C240 from 390pF to 470pF.
Change C254 from 820pF to 1000pF.
Change R273 from 28.7KR to 29.4KR.
Change C253 from I to NI.
Page 31: Change Q53.S from WAKE# to LAN_WAKE#.
Change Q53.D from LAN_WAKE# to WAKE#.
Page 37: Change C901 from NI to I for EMI suggestion.
Page 44: Change E25 footprint from 2X30_XDP_CONN_TEST to 2X30_XDP_CONN.

2017/07/19
Page 6: Change CPU1.AJ22 connection from VCCP to NA.
Page 32: Add C904.
Page 37: Change C901 from 100pF to 47pF.
Page 41: Add C905.

2017/07/20
Page 08: Remove R33,R709.
Change NET name from VDDSPD to VCC3.
Page 26: Change R340 from 10K to 11.5K.
board id : PV 0011
Page 36: Change R545 from NI to I.
Change R553 from I to NI.

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